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Using a logic analyzer to test an Atari 2600 ROM reader device

Lab Session[1]
Computer Structure

WARNING: A written solution of the preliminary work is required to carry out the laboratory session. A written solution will be presented per person and given to the instructor during the session. The solution must answer all the issues and must be detailed, complete, clear and well presented. The teacher can ask questions or seek clarification on the solution. Each student must bring a hard copy of this document.

1. Introduction

The logic analyzer is a laboratory instrument that greatly facilitates the testing of digital circuits and systems with a high number of inputs and outputs (direct access memories, for example). As oscilloscopes, logic analyzers use their channels to measure voltage, but there are remarkable differences:

- An oscilloscope can measure simultaneously a small number of signals (usually just 2), while a logic analyzer can read many of them simultaneously (usually tens of them).
- The oscilloscope measures continuous voltage levels, while the logic analyzer only sets if the signals are above or below a certain threshold. Thus, the analyzer can indicate the logical value of a signal (0 or 1), but can not specify its voltage.
- An oscilloscope continuously monitors and draws the input signals. The analyzer, however, only examines the signals at certain moments to register its logical value in an internal memory (the act of reading and recording the logic value of the signals is called capturing). The analyzer can only tell us the logical value of the inputs when they were captured.

Logic analyzers can make captures spaced in time at a selected frequency, for which they have an

internal clock. However, they can also be configured to make the captures when an edge on a special input (external clock input) happens. They can also be configured to start capturing when a specific pattern in the data channels is detected (this pattern is called 'trigger word').

The analyzer works as follows: first it captures iteratively the signals, storing its logic value in the analyzer internal memory; afterwards it pass the captured data to the PC, which will draw them on the screen and will provide us with timing measuring tools. Also, it will be possible to save the captured data to a file.

All this makes the analyzer an ideal tool for measuring and testing digital systems and buses.

The analyzer to be used in this session is a LA-2132. It is a PC-based logic analyzer, i.e. a small data capturing hardware that uses the PC for displaying. We will use it to analyze the behavior of a ROM reader system. It has been designed to read ROM memories of Atari 2600 cartridges. These memories have a size of 4KBytes, i.e. 2^{12}x8 bits. Each of the 4K memory locations will be read so every memory address (from 0 to 4095) will be generated. To this end, the ROM readers includes a 12-bit counter. The counter has been constructed by connecting 74191 chips. The 74191 component is a 4-bit counter triggered by the rising edge of the clock (see the appendix at the last page). A simplified schematic of the ROM reader circuit is shown in figure 1.

2. Goals

- Introducing the logic analyzer.
- Testing a simple digital circuit (the Atari 2600 ROM reader).
- Dumping a ROM and checking its correctness by using an Atari 2600 emulator.
- Measuring propagation delays and maximum operation frequencies.

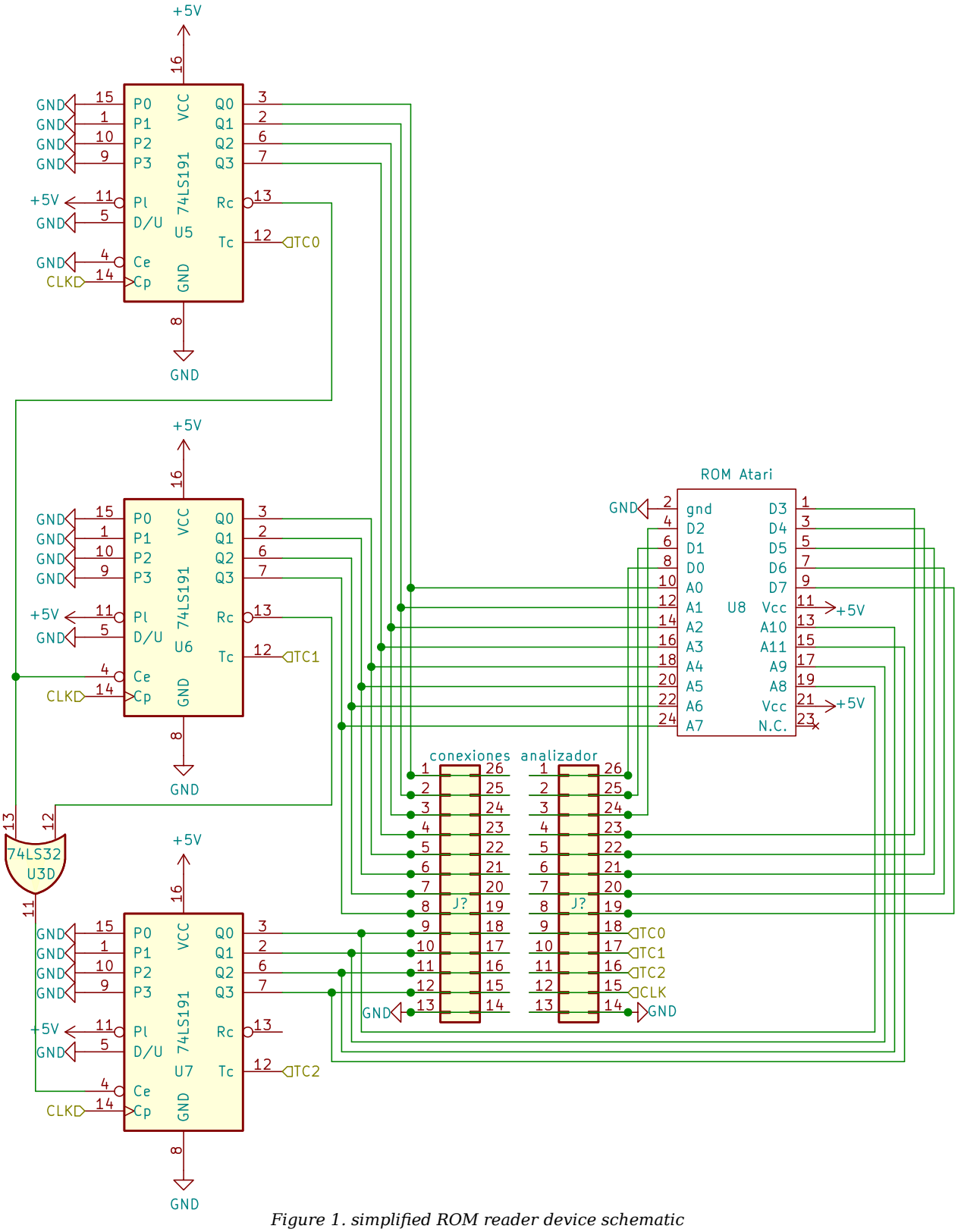
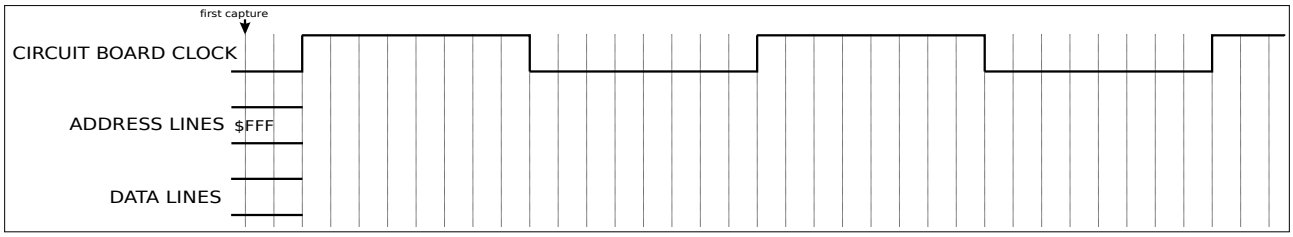


Figure 1. simplified ROM reader device schematic

3. Preliminary work

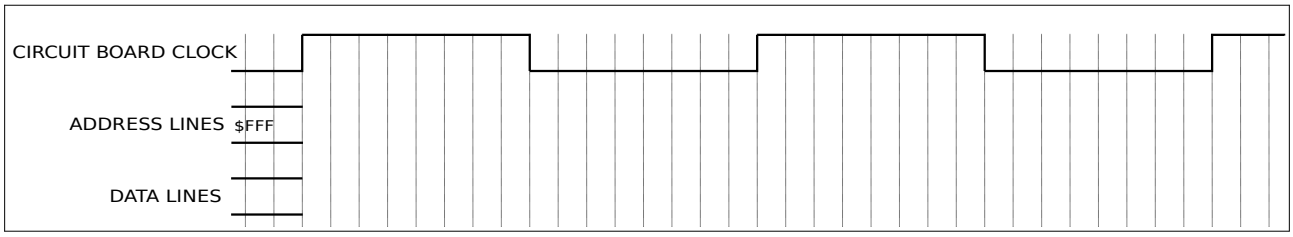
Study and understand the appendix describing the 74191 as well as the circuit of figure 1. After that, complete the following assignments:

1. Lets suppose that the content of the lowest memory locations ($000, $001 y $002) is $37, $A9 and $7E respectively, and that the content of the highest memory location is $00. Suppose also that the counter initial state is $FFF, and that every component has negligible delay. Complete the following chronogram:



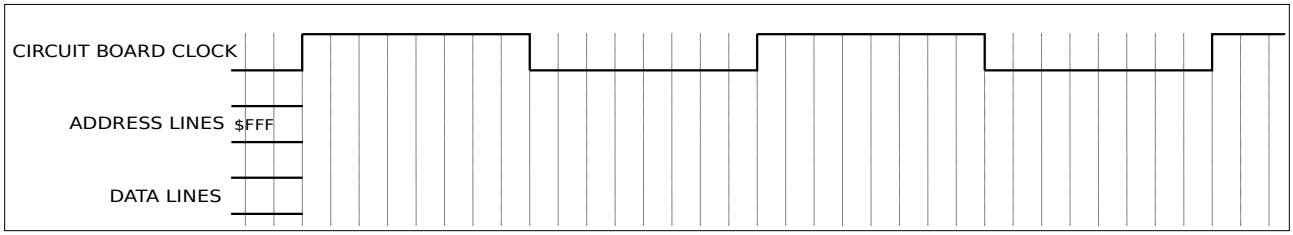
2. For the previous chronogram, suppose that the logic analyzer captures data at a frequency four times higher than the circuit board clock frequency. Suppose also that the first capture happens at the instant marked with an arrow. Mark in the chronogram the instants when the other captures are carried out and write down **in a table** the value of the data and address lines in each capture.

3. Complete again the following chronogram, but suppose now that the counter has a delay $R_c>0$ and the ROM a delay $R_r>0$. Suppose also that the sum of both delays is shorter than a half the period of the board clock (i.e. $R_c+R_r < T_p/2$, where T_p is the board clock period). **Do not forget to highlight each component delay.**



4. For the previous chronogram, write down **in a table** the data and address values that would be captured if the logic analyzer is configured to capture at the falling edge of the circuit board clock.

5. Complete again the following chronogram supposing that both delays are shorter than a half the period of the board clock, but its sum is longer ($R_c < T_p/2$, $R_r < T_p/2$, $R_c+R_r > T_p/2$). **Do not forget to highlight each component delay.**



6. For the previous chronogram, write down **in a table** the data and address values that would be captured if the logic analyzer is configured to capture at the falling edge of the circuit board clock.

7. For the previous chronogram, write down **in a table** the data and address values that would be captured if the logic analyzer is configured to capture at the rising edge of the circuit board clock.

(a)

Analyzer pin	Wire color	Reader pin
0	brown	D0
1	red	D1
2	orange	D2
3	yellow	D3
4	green	D4
5	blue	D5
6	magenta	D6
7	gray	D7
8	brown	A0
9	red	A1
10	orange	A2
11	yellow	A3
12	green	A4
13	blue	A5
14	magenta	A6
15	gray	A7
16	brown	A8
17	red	A9
18	orange	A10
19	yellow	A11
20	green	FC0
21	blue	FC1
22	magenta	FC2
GND	black	GND
31	gray	CLK

(b)

Figure 2. (a) Connectors and component layout, (b) connection table

4. Lab work

The ROM reader has been implemented in a Printed Circuit Board (PCB). Apart from that PCB, the following items are required to carry out the lab session: Logic analyzer, wave generator, oscilloscope and Atari 2600 cartridge. The latter contains another PCB with the ROM. The oscilloscope will be used just to check the clock signal.

4.1. Connecting the equipment.

The PCBs are shown in figure 2a. The ROM reader includes the following:

- A connector to plug the Atari 2600 ROM PCB. The ROM will be always active so the content of the addressed memory location will be always shown at the ROM output (signals from D0 to D7).
- Three 4-bit counters model 74191 and an OR gate model 7432 connected to form a 12-bit counter. Its count state output is connected to ROM address lines.
- An USB-B connector to provide the supply voltage of the circuit.
- A coaxial connector to connect the clock signal.
- Two pin rows to connect the logic analyzer. They are connected through the PCB to the address lines, the data lines, the terminal count signals (TC0, TC1 and TC2), the clock signal and ground.
- Capacitors for decoupling the supply.

Before connecting the circuit board to the supply voltage (DC voltage source) you must do the following:

1. First extract the ROM PCB from the cartridge and insert it into the reader socket. DO NOT INSERT THE ROM PCB BACKWARDS: The side with the ROM goes up.
2. Connect the probes and the ground of the logic analyzer to the pin rows as indicated in the table of figure 2b.
3. Use the wave generator to get the clock signal. It must be a square signal swinging between 0 and 5 volts at a frequency of 25 Khz. The duty cycle must be 1/2, i.e. during each cycle the signal must be at the high value for a half the period and at the low value for a half the period. You will have to use the oscilloscope to make sure that the signal is O.K.

Only after having carried out the previous steps you will have to connect the supply and the clock signal to the circuit board. To do so you will need some of the USB-B cables connected to the PC and a coaxial cable. After this the ROM will show in the data lines the content of each of its memory locations sequentially.

4.2. Setting the LA-2132 to check the circuit board

Note that you must connect the analyzer to your PC before executing the LA-2132 software. This software, available for Windows, can be executed by clicking on the O2164.exe icon of the desktop.
The application window has several components. The upper frame contains several menus (File, View, Timing,...). Bellow it there is a row of commands to be executed (Go, Stop, ...). The lower frame has two parts:

- The upper part contains the controls for the system cursors, the zoom and a bar to move along the captured data.
- The lower part is used to display the captured data.

Before capturing and watching the signals you will have to set up the logic analyzer. To do so, right-click on the lower part. The parameters window depicted at figure 3 will emerge. Change its fields as follows:

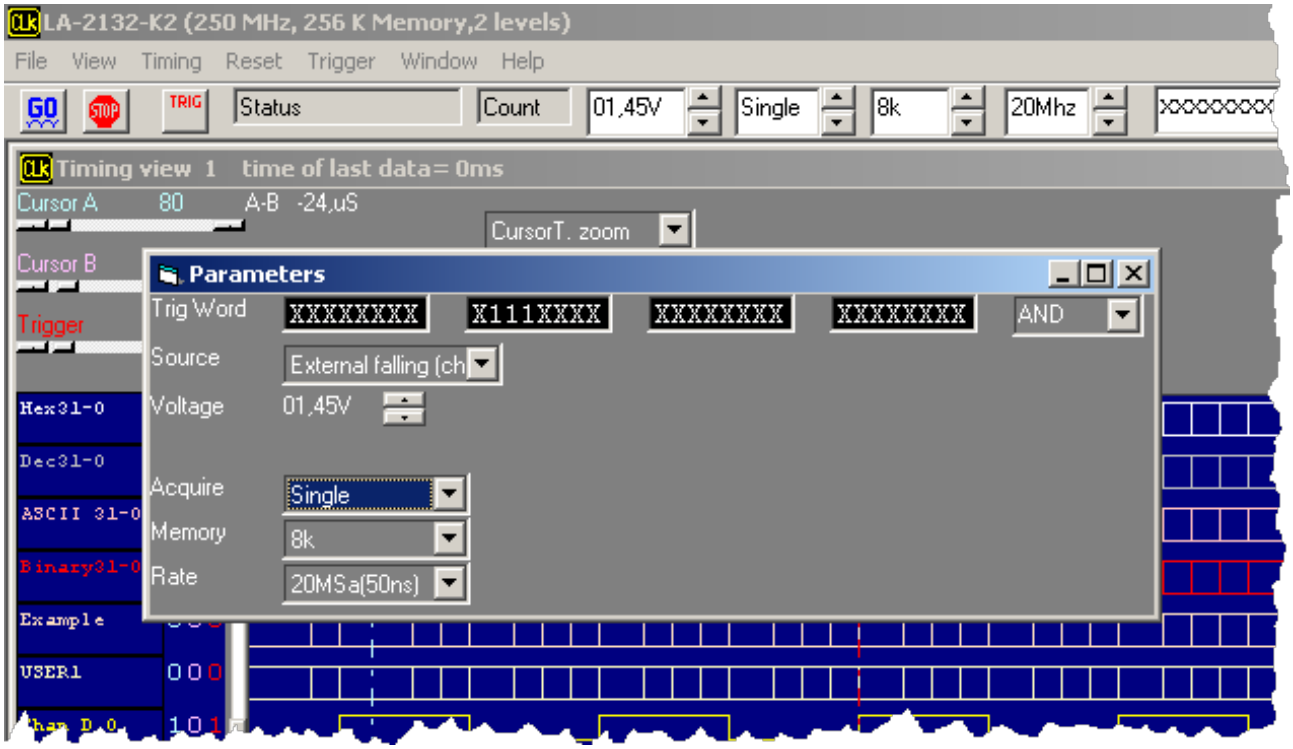


Figure 3. Parameters window

En la ventana *Parameters* recién aparecida, seleccionamos las siguientes opciones:

- In the field Trig Word enter '1' in the places for the channels 20, 21 and 22, i.e. the channels measuring terminal count signals (within the field the channel order is 31, 30, 29, .., 0). This way we will tell the analyzer when to start sampling (the count state is $FFF if all the terminal count signals are equal to 1).

- In the field Source choose External falling. This way the captures will be carried out at the falling edge of the external clock, i.e. the circuit board clock.

- Choose 8K in the field Memory so only 8K samples will be recorded.

- Choose Single in the field Acquire so the analyzer will stop after taken the 8K samples.

Close the parameters window. Now the logic analyzer is set up to start sampling when all the terminal count signals are equal to 1, i.e. when the address lines are equal to $FFF. It is better if the analyzer starts sampling when the address lines are equal to $000, i.e. just when the triggering condition changes from true to false. For so, click on the Trigger button and, on the emerging window, look for line Level 0 and change the field from Enter to Exit. After this close the emerging window.

The last task is grouping the channels. To do so click on View → Group edit The window depicted at figure 4 will emerge. For each channel group we must enter its name, the numeric base that will be used to represent the values, the number of channels within the group and finally which channels form the group. The latter is defined in the table of figure 2b. You must define the following groups:

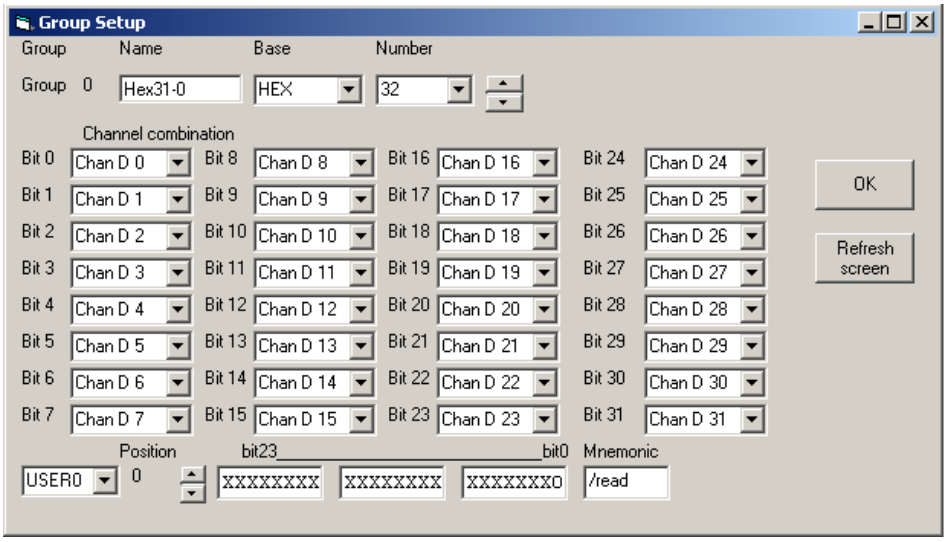


Figure 4. Group Setup window

1. The first one, called 'content', will be the group of channels measuring the ROM output and will be shown in hex.

2. The second one, called 'address', will contain the channels measuring the counter state and will be also shown in hex.

3. The third one, called 'End of Count', will contain the channels measuring the TC signal of each 74191 and will be shown in binary.

4. The fourth one, called 'clock', will contain just the circuit board clock (channel 31) and will be shown in binary.

As an example figure 5 shows the window after setting group 2.

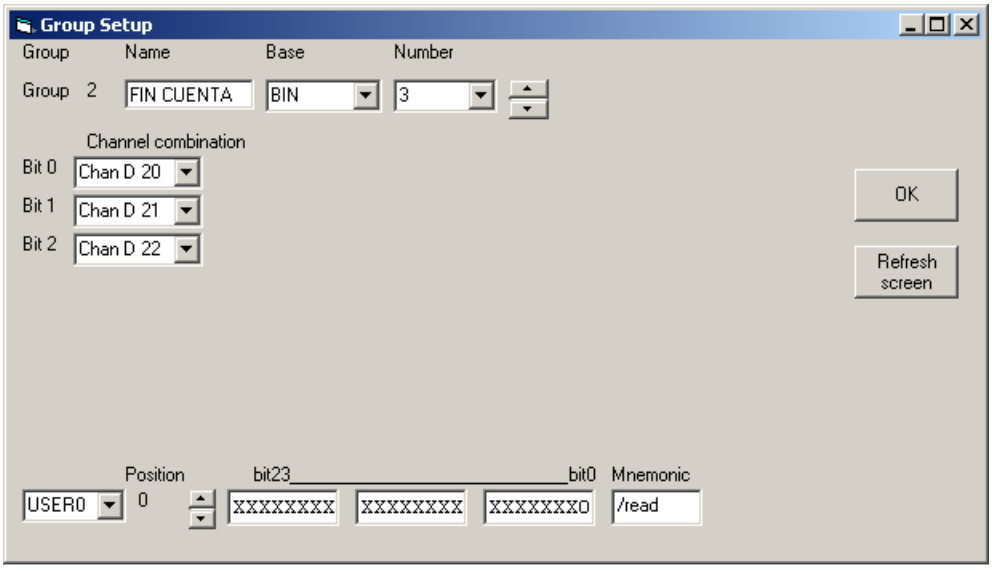


Figure 5. Group 2 setting.

Now the analyzer is ready to acquire data. Just click on the GO button and the process will start. Once the 8K samples have been carried out, the data will be shown on screen. To make sure that everything was correct check the following:

- The value coded in the address lines must be an unit higher in each capture since they are the output of a counter. Their waveforms must be square signals, and the period of each one must be twice the period of the previous one.
- The TC signals must be high simultaneously only when the counter reaches the last state, i.e. $FFF.

You must also check that the content of each memory location is shown sequentially at the ROM output. Since the ROM comes from an Atari 2600 cartridge, this can be checked by saving the captured data and using an Atari 2600 emulator to execute it as described below:

1. For saving the capture you must do the following:
   1.1. In the LA-2132 software menu click on File → Save data → Save data as.
2. Select the folder C:\Users\practicas and choose the filename *captura*. Click on Guardar.
3. Now we must extract the data corresponding to the ROM output from the file and save it into a binary file (the ROM image file). For creating the ROM image file do the following:
   3.1. Open a command line window. This can be carried out in the following ways:
      - In Windows XP and Windows 7 click on Inicio→ Todos los programas → Accesorios → Símbolo del sistema.
      - In Windows 10 right-click on Inicio and select WindowsPowerShell. Alternatively you can search and execute the cmd command.
   3.2. Execute the following commands

```
cd c:\users\practicas
dso2bin captura.dso juego.bin
```

   The first command changes the working directory and the second one writes the ROM image file.
4. In order to check the dump with the Stella emulator do the following:
   4.1. Double-click on the Stella icon on the desktop.
   4.2. Within the emulator, double-click on the juego.bin image file you have just created.
   4.3. Make sure the Atari 2600 program works. The main keys are F2 (start), space (fire), and the cursor keys.

4.3. Checking the correctness of the preliminary work

1. Click on View → State of logic analyzer. to see the samples list. Click on the T button to see the sample which triggered the capturing process. Write down some of the memory address captured and their corresponding memory location content. In particular, write down the content of the memory locations $000, $001, $002 and $003.
2. Change the analyzer setting so it will capture data at four times the frequency of the circuit board clock . To this end, open again the *Parameters* window and select Internal in the field Source and 100KSa(10us) in the field Rate Check your answer to question 2 of the preliminary work.
3. Change the analyzer internal clock frequency to 250MSa(4ns) and capture again. Measure the counter delay (R_c) and the ROM delay (R_r) using the cursors.
4. To check your answer to questions 5 and 6 of the previous work to the following:
   4.1. Open again the *Parameters* window and select External falling in the field Source and Auto in the field Acquire so the analyzer will capture iteratively without stopping.
   4.2. Click on GO to start the process, click on 'View → State of logic analyzer and click on the T button to see the sample which triggered the capturing process.
   4.3. Increase slowly the circuit board clock frequency. Stop just when the data you wrote down in step 1 are not displayed correctly anymore.
   4.4. Calculate the circuit board clock period and check the inequality of question 6 of the previous work.
5. Change the analyzer setting again so it will capture data at the rising edge of the circuit board clock. To do so select External rising in the field Source of the *Parameters* window. Use the data you wrote down in step 1 to check your answer to question 7 of the previous work.

Appendix: 74191 four-bit counter description

The 74191 component is a four-bit counter with the following input/output signals:

- Q (Count State, output): Four lines showing the state of the counter registers.
- P (Parallel Load, input): Four lines used to specify the next state of the counter when parallel loads are carried out.
- CE (Count Enable, input): used to enable the counting process (active at the low level).
- U/D (Up/Down, input): used to choose counting up (0) or counting down (1).
- CP (Clock Pulse, input): is the clock signal for the counter registers. They are triggered by the rising edge.
- TC (Terminal Count, output): it is active only when the counter is at the last state (1111).
- RC (Ripple Clock, output): If CE is disabled or the counter is not in the last state is equal to 1. Otherwise is equal to CP.
- PL (Parallel Load, input): when it is equal to zero the counter carries out a parallel load.