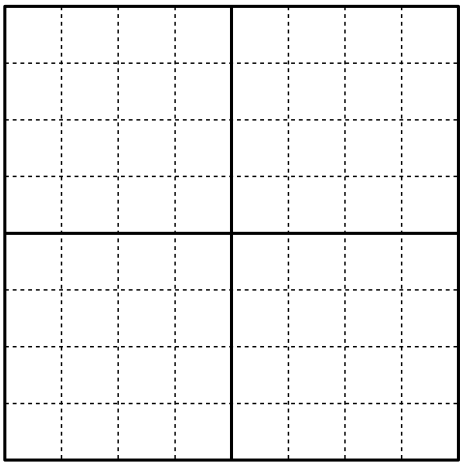
Digital Electronic Circuits

Laboratory session 1

Introduction to the digital laboratory

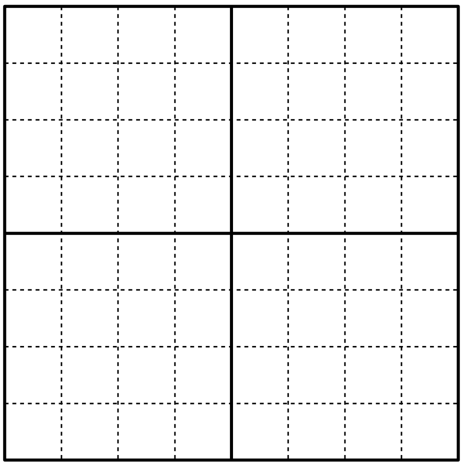
1. Obtain the following signals from the power supply and visualize them in the oscilloscope.
   a) +5V DC signal
   b) +10V DC signal
   c) -10V DC signal

(a)



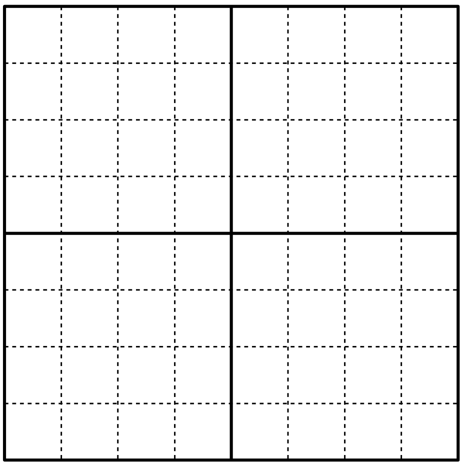
v. scale ____________ t. scale ____________

(b)



v. scale ____________ t. scale ____________

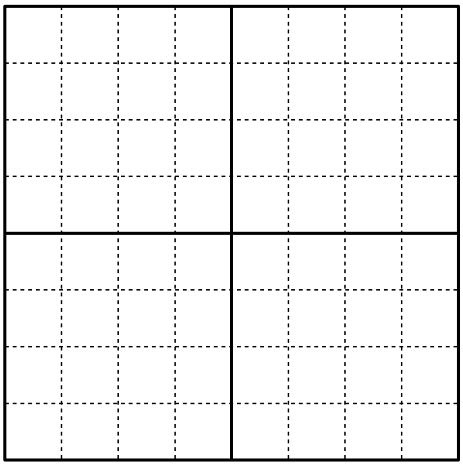
(c)



v. scale ____________ t. scale ____________

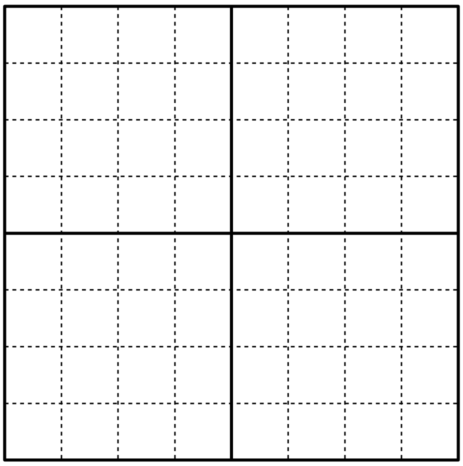
2. Obtain the following signals from the function generator and visualize them in the oscilloscope.
   a) Sine signal from -5V to +5V, f=1kHz
   b) Ramp signal from -7V to +3V, f=10kHz
   c) Square signal from 0V to 5V, f=100kHz

(a)



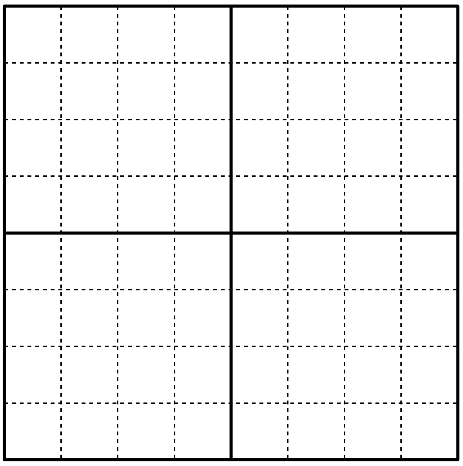
v. scale ____________ t. scale ____________

(b)



v. scale ____________ t. scale ____________

(c)

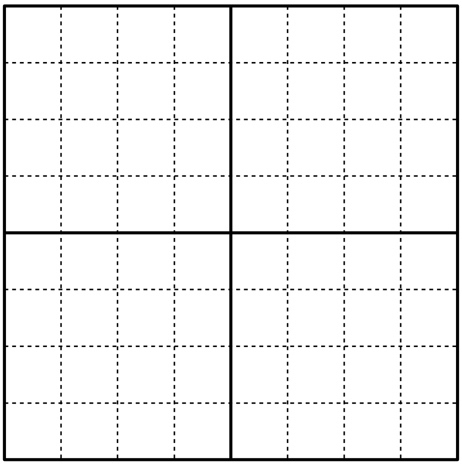


v. scale ____________ t. scale ____________

3. Test a NAND gate from a 7400 chip (pin-out at the end of this document) using an LED and a current-limiting resistor. Measure the voltage at the output of the gate for every input combination. Take note of the results and compare with the expected truth table of the gate.
4. Test a NAND gate from a 7400 chip using a waveform generator and oscilloscope (see sample illustration at the end of this document). Use a 100kHz square signal. Consider the following cases:
   a) $x = 0$, y = square signal.
   b) $x = 1$, y = square signal.
   c) $y = 0$, x = square signal.
   d) $y = 1$, x= square signal.

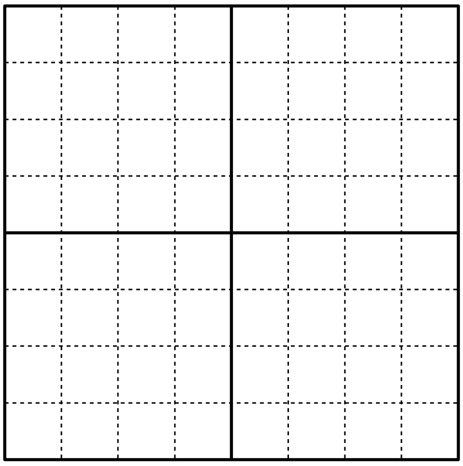
   Deduce the truth table of the NAND gate from the results and compare with the expected table.

(a)



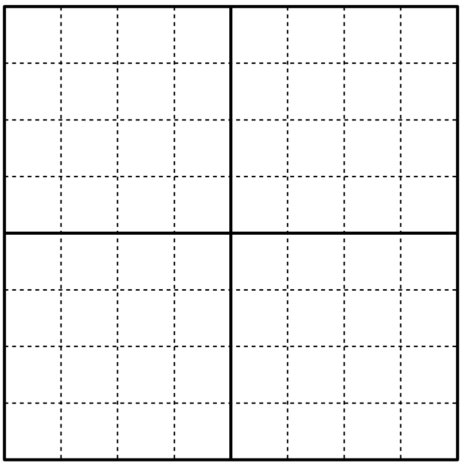
v. scale ____________ t. scale ____________

(b)



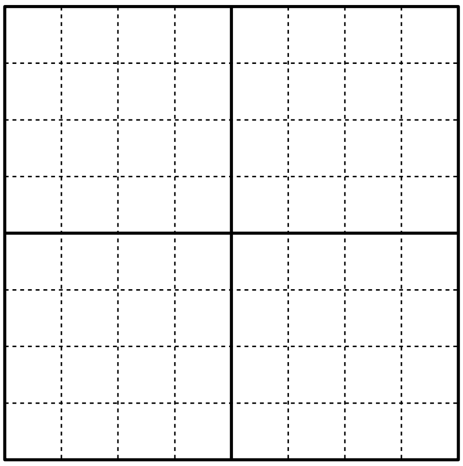
v. scale ____________ t. scale ____________

(c)



v. scale ____________ t. scale ____________

(d)



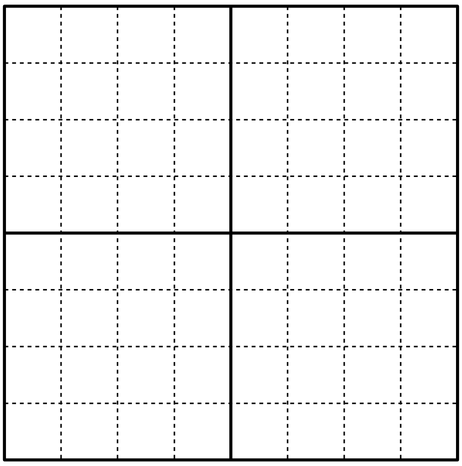
v. scale ____________ t. scale ____________

5. Calculate the time characteristics of the NAND gate. Use y = 1 and a squared signal in x. Connect the output of the gate under test to the input of another gate in the same chip (see sample illustration at the end of this document).

   a) Delay time: t_{pHL}, t_{pLH}.

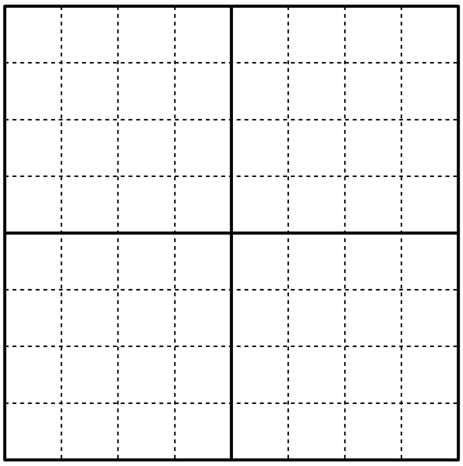
   b) Output transition time: t_{HL}, t_{LH}.

t_{pHL}



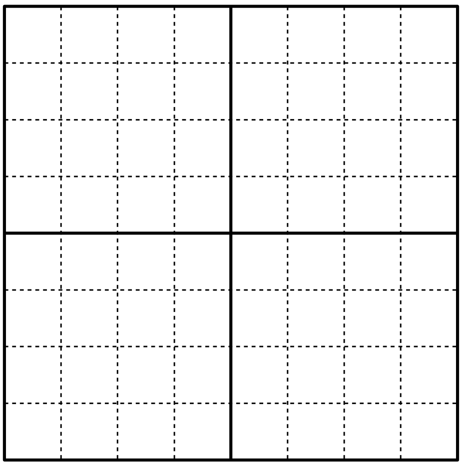
v. scale ____________ t. scale ____________

t_{pLH}



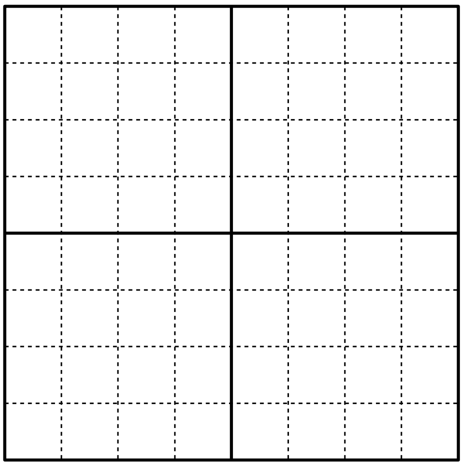
v. scale ____________ t. scale ____________

t_{HL}

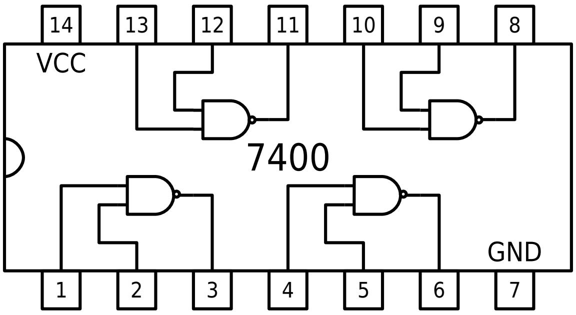


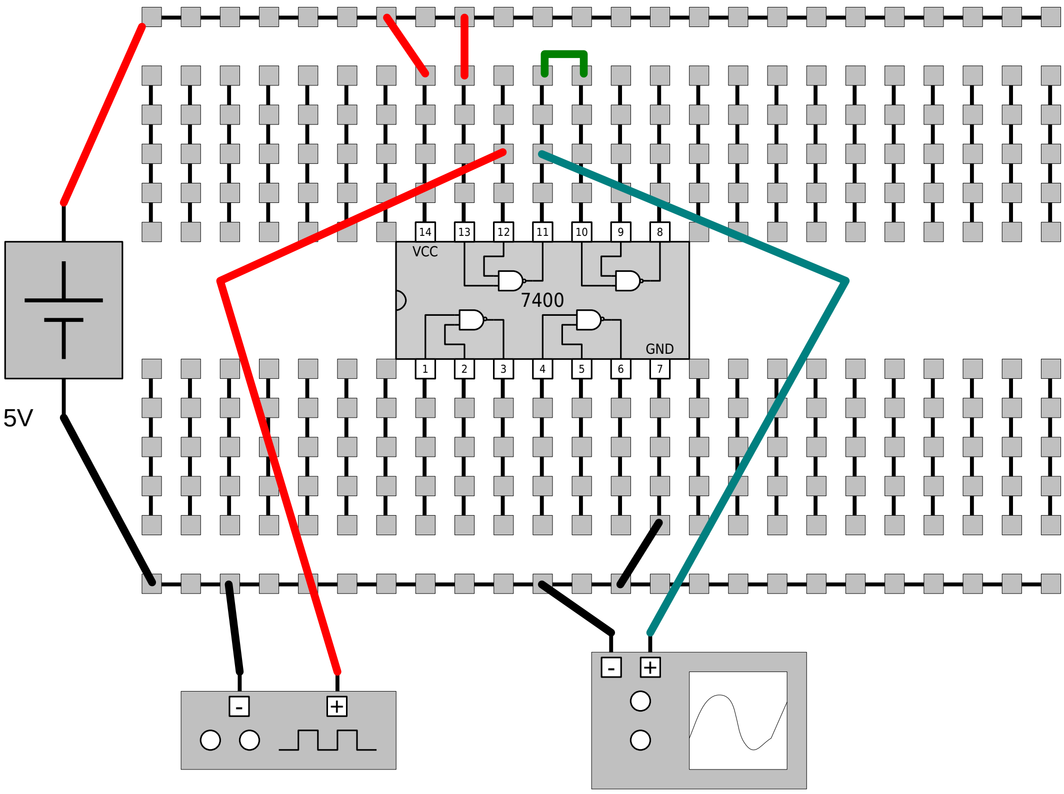
v. scale ____________ t. scale ____________

t_{LH}



v. scale ____________ t. scale ____________


14
13
12
11
10
9
8
VCC
7400
GND
1
2
3
4
5
6
7


14
13
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VCC
7400
GND
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3
4
5
6
7
5V
-
+
-
+