Assignment 5

Exercise 1. Design an arithmetic circuit with an 8-bit input signal 'x' and an 8-bit output 'z' signal so that z = (x + 79) mod 256. Use basic adder blocks (full adders –FA– and half adders –HA–). Add an overflow output 'c'.

Exercise 2. Design an arithmetic circuit with an 8-bit input signal 'x' and an 8-bit output 'z' signal so that z = (6 * x) mod 256. Use basic adder blocks (full adders and half adders). Add an overflow output 'c'.

Exercise 3. Do the following arithmetic operations in binary using two's complement notation and check that the result is correct using decimal arithmetic. For each case use the minimum number of bits that will give a correct result.

a) (+42) + (-13) b) (+42)-(-13) c) (-42)+(-13) d) (-42)-(-13)

Exercise 4. Design and test the following arithmetic circuits in circuitjs simulator[1]. Use a 4-bit magnitude adder[2] as starting point.

a) An 8-bit two's complement adder with an overflow output (no carry input).

b) A 4-bit two's complement adder/subtractor with an overflow output.

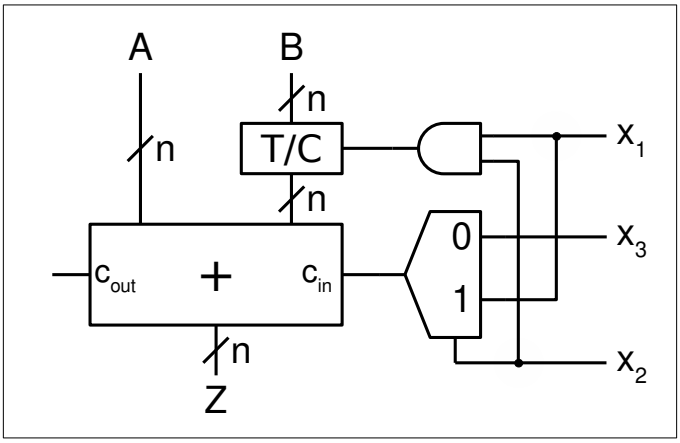
Exercise 5. Design an 8 bit signed/unsigned adder with an overflow output 'v'. Overflow should indicate an incorrect result considering the type of data (signed or unsigned). Circuit ports are:

- a, b: data inputs
- u: data type input (0-signed, 1-unsigned)
- z: data output
- v: overflow output

a) Implement the circuit using FA, HA and other gates or subsystems.

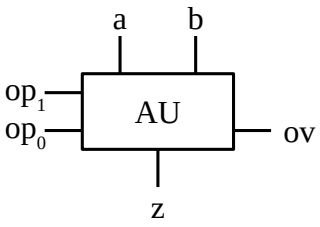
b) Write a Verilog description, an adequate test bench and simulate the circuit until it is correct.

Exercise 6. The circuit in the figure includes a n-bit magnitude adder (+) and a transfer/complement block (T/C) among other devices. Describe the operation of the circuit by using an operation table and a word description.



Exercise 7. Design an n-bit arithmetic unit with input 'a' and 'b' and output 'z' as shown in the table and figure, including a two's complement overflow signal 'v'. Use basic adder blocks (FA and HA), combinational subsystems and logic gates at your own convenience.

1 http://lushprojects.com/circuitjs/circuitjs.html
2 https://tinyurl.com/yxqunzup



op[1:0]	z
00	a - b
01	b - a
10	a + 1
11	b

Exercise 8. Design a two's complement ALU with the operations in the table. Include carry (c) and overflow (v) outputs.

a) Implement it using FA, HA and other gates or subsystems.

b) Write a Verilog description, an adequate test bench and simulate the circuit.

op[2:0]	Operation	z
000	Addition	a + b
001	Substraction	a - b
010	Increment 2	a + 2
011	Decrement 2	a - 2
100	AND	a AND b
101	OR	a OR 2
110	XOR	a XOR 4
111	Complement	NOT a