Last Name, Name: _____

# *Simple computer 2*

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## 1 Material

- Computer with Xilinx ISE 14.x installed.
- A Basys2 development board and documentation. It includes a Xilinx Spartan-3E FPGA.
- YASAC simple computer Verilog files.

## 2 Description

The goal of this lab is to learn to modify, fix bug and do some practical programming on the YASAC Stage 5 computer described in unit 4 of the course in a Basys2 development board. You can find the top-level schematic of the system and additional details in the course's slides and other course's material.

## 3 Learning Outcomes

- Understand the structure and implementation of a simple computer.
- Write simple test programs in assembly code and translate them to machine code.
- Modify the design of a simple computer to implement new instructions.
- Debug a simple computer Verilog description to find and fix design errors.

## 4 Pre-lab

1. There is a bug in the definition of the YASAC's BRCC pseudo-instruction in the Verilog code. Find and fix it.
2. Write a program for YASAC Stage 5 that reads a value *n* from port08 and generates the first *n* terms of the Fibonacci sequence with 8 bits. Each term is output in port01 as it is generated so it will be displayed in the seven segment display of the YASAC system.
3. Modify the default test bench if necessary and simulate your code to check that it is correct.

# 5 Lab work

1. Implement the system including your program in the development board and check that it works correctly.
2. What is the maximum number of terms that can be generated correctly with an 8-bit result?