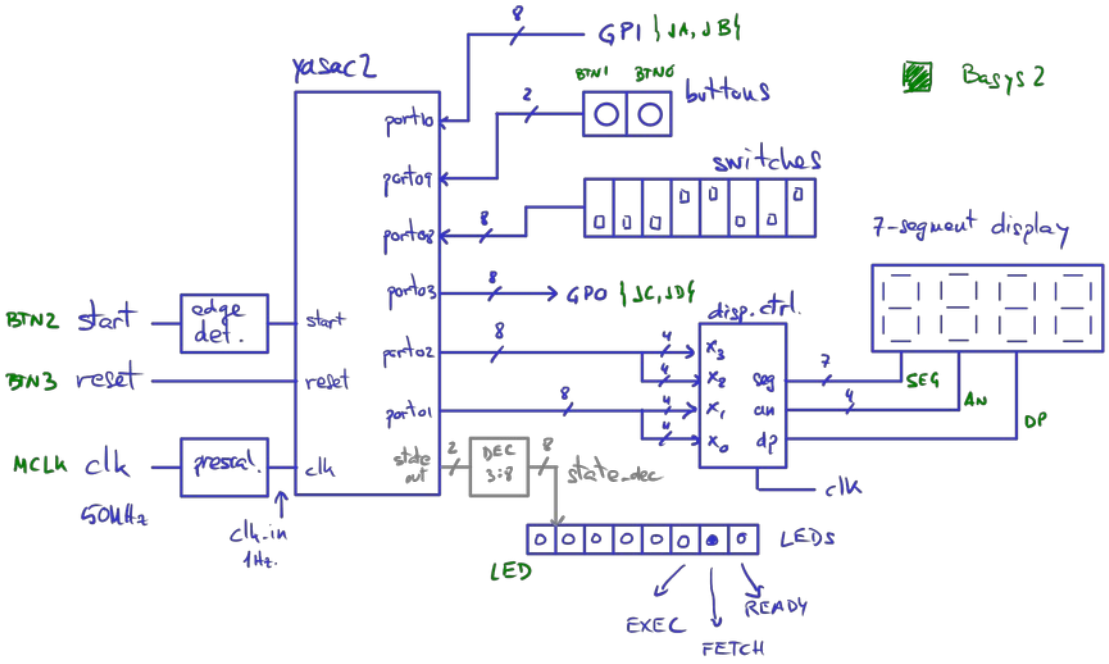
YASAC Cheat Sheet, March 2023

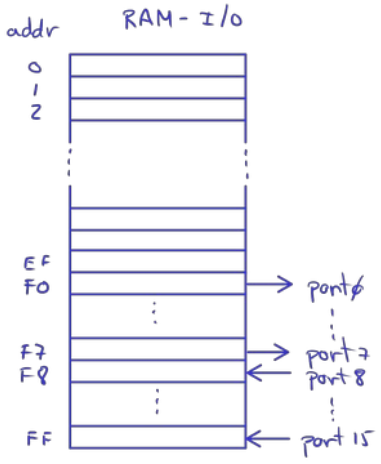
YASAC System on Chip

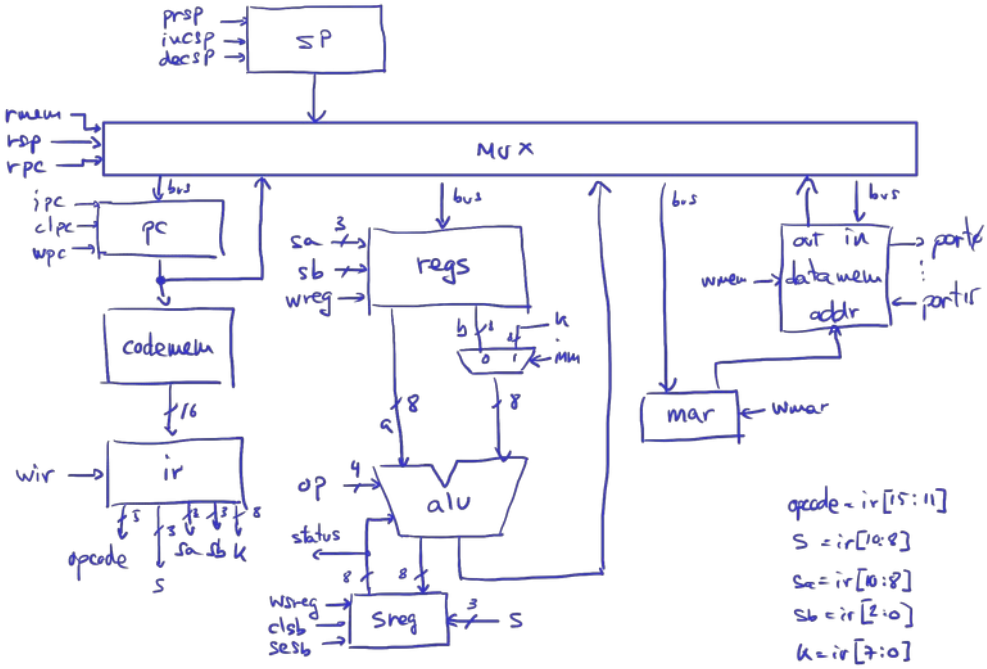


YASAC Data Unit

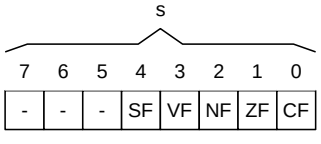
regs

R0
R1
R2
R3
R4
R5
R6
R7





sreg



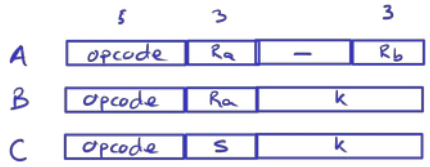
Status register flags

- CF: Carry Flag
- ZF: Zero Flag
- NF: Negative Flag
- VF: oVerflow Flag
- SF: Sign Flag

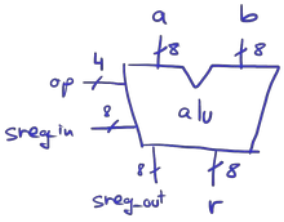
YASAC Instructions

Op. code	Instruction	RTL	SVNZC
00001	LDI Ra,k	Ra ← k	-----
00010	MOV Ra,Rb	Ra ← Rb	-----
00011	ADD Ra,Rb	Ra ← Ra+Rb	*****
00100	SUB Ra,Rb	Ra ← Ra-Rb	*****
00101	STOP	–	-----
00110	LD Ra,Rb	Ra ← datamem(Rb)	-----
00111	ST Rb,Ra	datamem(Rb) ← Ra	-----
01000	LDS Ra,k	Ra ← datamem(k)	-----
01001	STS k,Ra	datamem(k) ← Ra	-----
01010	JMP k	PC ← k	-----
01011	BRBS s,k	status[s]: PC ← k	-----
01100	BRBC s,k	~status[s]: PC ← k	-----
01101	AND Ra,Rb	Ra ← Ra & Rb	*****
01110	OR Ra,Rb	Ra ← Ra | Rb	*****
01111	EOR Ra,Rb	Ra ← Ra ^ Rb	*****
10000	ROR Ra	Ra ← SHR(Ra,C)	*****
10001	ROL Ra	Ra ← SHL(Ra,C)	*****
10010	BCLR s	sreg[s] ← 0	*****
10011	BSET s	sreg[s] ← 1	*****
10100	PUSH Ra	datamem[sp] ← Ra; sp ← sp - 1	-----
10101	POP Ra	Ra ← datamem[sp+1]; sp ← sp + 1	-----
10110	CALL k	datamem[sp] ← pc; pc ← k; sp ← sp - 1	-----
10111	RET	pc ← datamem[sp+1]; sp ← sp + 1	-----

Instruction formats



ALU operations



sreg

OP Sym.	OP	r	S V N Z C
ALU_ADD	0 0 0 0	a+b	* * * * *
ALU_TRA	0 0 0 1	a	- - - - -
ALU_SUB	0 0 1 0	a-b	* * * * *
ALU_TRB	0 0 1 1	b	- - - - -
ALU_NEG	0 1 0 0	-a	* * * * *
ALU_AND	0 1 0 1	AND(a,b)	* * * * -
ALU_OR	0 1 1 0	OR(a,b)	* * * * -
ALU_EOR	0 1 1 1	EOR(a,b)	* * * * -
ALU_ROR	1 0 0 0	SHR(a,c_{in})	* * * * *
ALU_ROL	1 0 0 1	SHL(a,c_{in})	* * * * *

Branch pseudo-instructions

Instruction	Pseudo-instructions	Description
BRBS 0,k	BRCS k BRLO k	Branch if carry (Carry Set) Branch if A<B after unsigned A-B (LOwer)
BRBS 1,k	BRZS k BREQ k	Branch if the result is zero (Zero Set) Branch if A=B after A-B (EQual)
BRBS 2,k	BRMI k	Branch if the sign is Minus
BRBS 3,k	BRVS k	Branch if overflow (oVerflow Set)
BRBS 4,k	BRLT k	Branch A<B after signed A-B (Less Than)
BRBC 0,k	BRCC k BRSH k	Branch if no carry (Carry Cleared) Branch if A≥B after uns. A-B (Same or Higher)
BRBC 1,k	BRZC k BRNE k	Branch if the result is not zero (Zero Cleared) Branch if A≠B after A-B (Not Equal)
BRBC 2,k	BRPL k	Branch if the sign is PLus
BRBC 3,k	BRVC k	Branch if not overflow (oVerflow Cleared)
BRBC 4,k	BRGE k	Branch A≥B after signed A-B (Greater or Equal)

Status pseudo-instructions

Instruction	Pseudo-instructions	Description
BCLR 0	CLC	CLear Carry bit
BCLR 1	CLZ	CLear Zero bit
BCLR 2	CLN	CLear Negative bit
BCLR 3	CLV	CLear oVerflow bit
BCLR 4	CLS	CLear Sign bit
BSET 0	SEC	SEt Carry bit
BSET 1	SEZ	SEt Zero bit
BSET 2	SEN	SEt Negative bit
BSET 3	SEV	SEt oVerflow bit
BSET 4	SES	SEt Sign bit