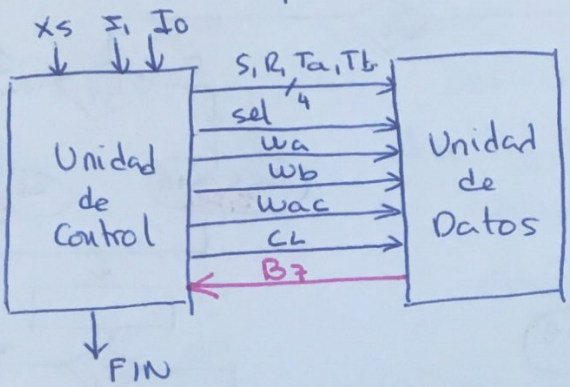
Prueba 1 EdC

Curso 2018/19

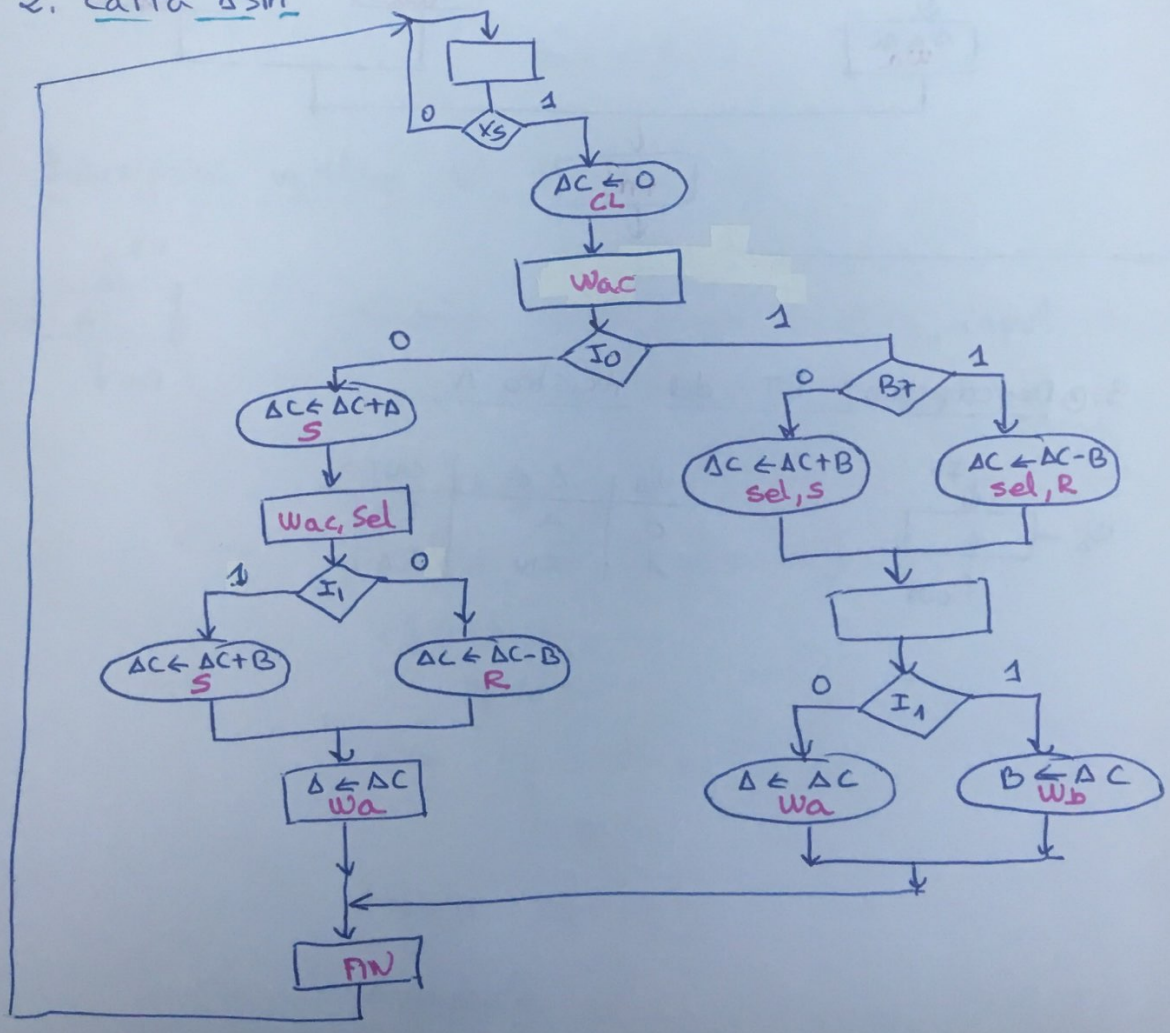
Problema 1 → consultar teoría (transparencias, apuntes, ...)

Problema 2

1. Diagrama de bloques

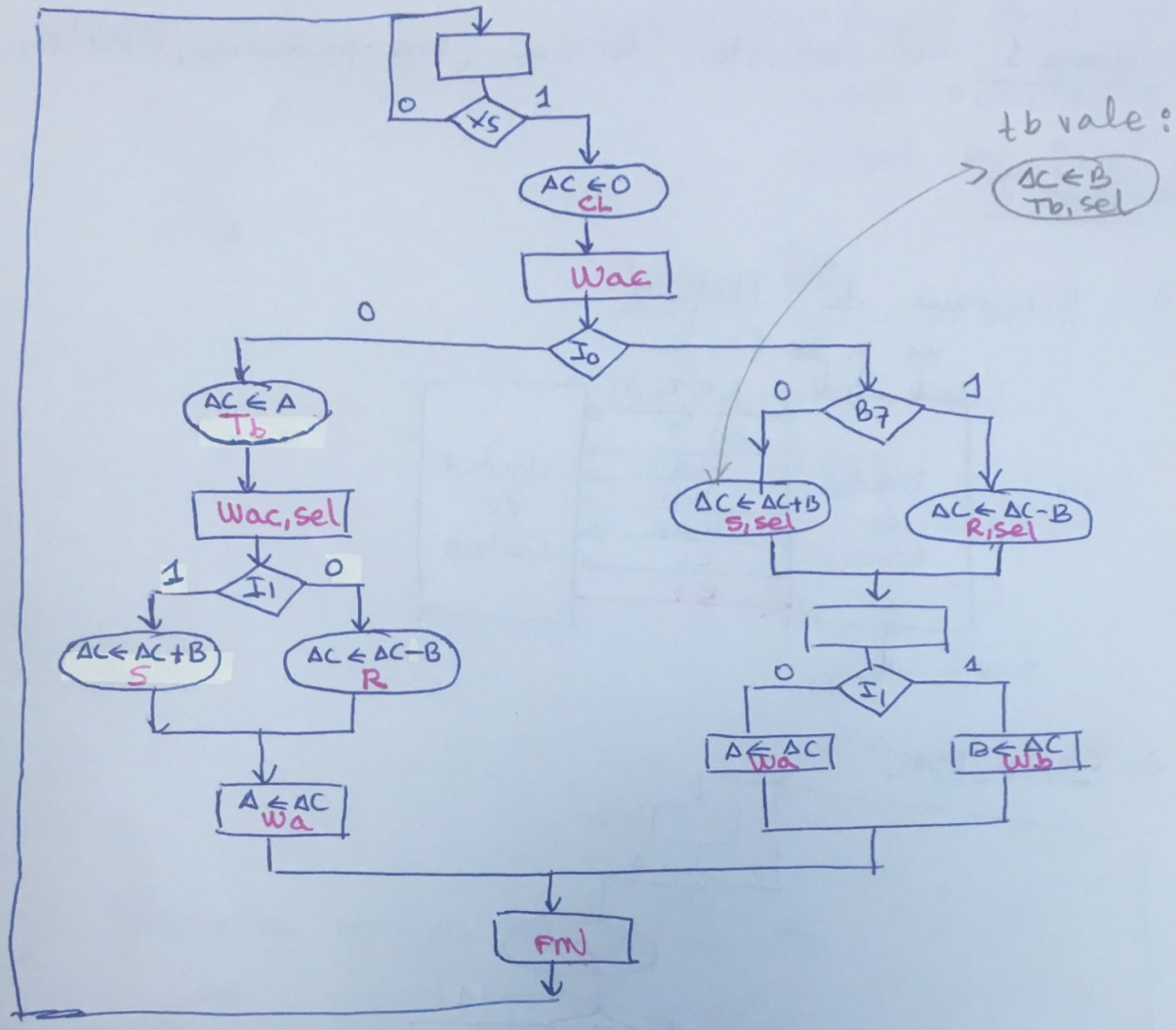


2. Carta ASM

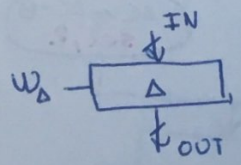


Scanned with CamScanner

Otra poible solución parc la carta ASM:



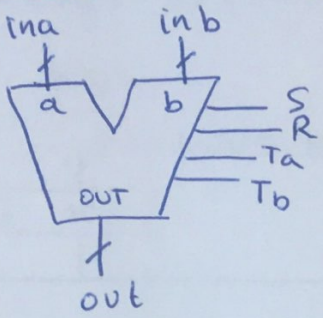
3. Descripción RT del registro A:



W_A	A ←	OUT =
0	A	[A]
1	IN	[A]

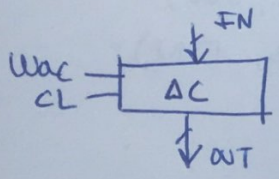
Scanned with CamScanner

Descripción - Verilog de la ALU




```
module ALU (input [7:0] ina, inb,
            input S, R, Ta, Tb,
            output reg [7:0] out);

always @*
  if (S)
     OUT = ina + inb;
  else if (R)
       OUT = ina - inb;
     else if (Ta)
          OUT = ina;
        else OUT = inb;

endmodule
```

Descripción verilog del registro AC

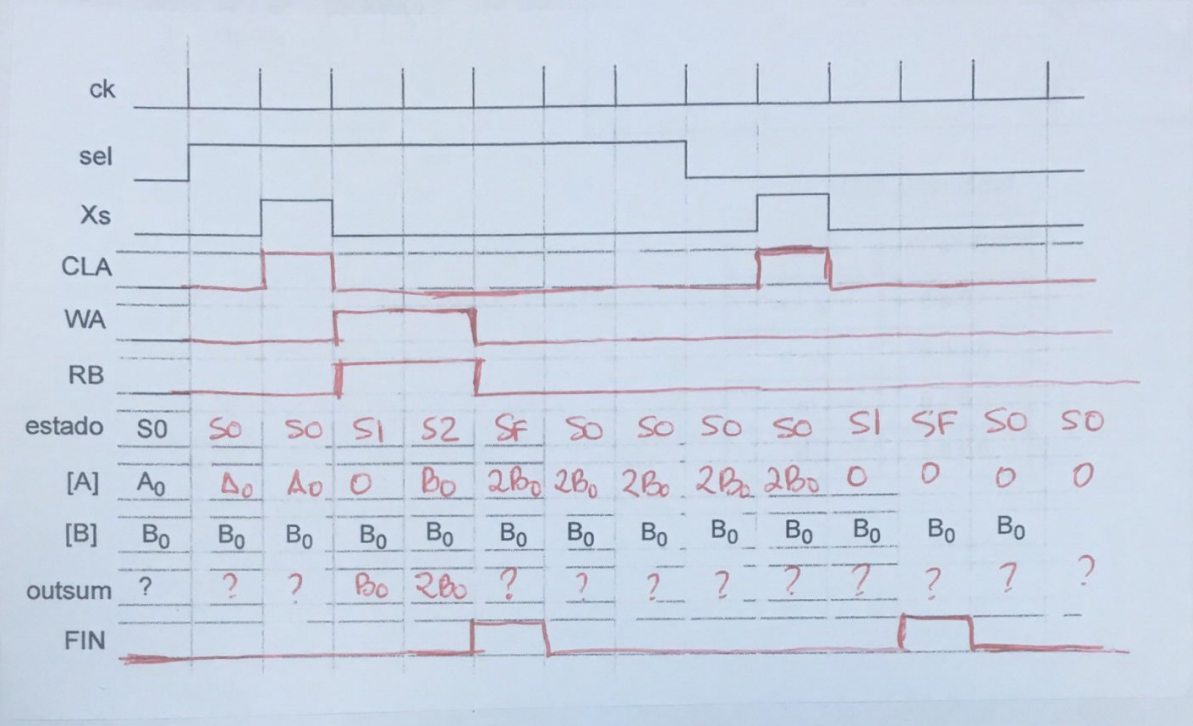



```
module regAC (input [7:0] in, input Wac, CL, CK,
              output [7:0] out);

reg [7:0] q;
always @ (posedge CK)
 if (cl)
    q <= 0;
 else if (wac)
      q <= in;

assign out = q;

endmodule
```

Scanned with CamScanner

Problema 3

1. Diagrama temporal



2. Descripción Verilog de la carta ASM

```
module unidad_de_control (input clk, reset, xs, sel,
                          output CLA, WA, RB, FIN);

parameter S0 = 2'b00, S1 = 2'b01, S2 = 2'b10;
reg [1:0] current_state, next_state;
always @ (posedge clk, posedge reset)
  begin
    if (reset)
      current_state = S0;
    else
      current_state = next_state;
  end
```

Scanned with CamScanner

```
always @(current_state, xs, sel)
  begin
    {CLD, WD, RB, FIN} = 0;
    case (current_state)
      S0: begin
          if (xs) begin
                  CLD = 1;
                  next_state = S1;
                  end
          else    next_state = S0;
          end
      S1: begin
          if (sel) begin
                  WD = 1;
                  RB = 1;
                  next_state = S2;
                  end
          end
      S2: begin
          WD = 1;
          RB = 1;
          next_state = SF;
          end
      SF: begin
          FIN = 1;
          next_state = S0;
          end
    endcase
  end
endmodule.
```

Scanned with CamScanner