```
module udatos  #(parameter N=8) (
   input ck,
   input W,
   input P1,
   input P0,
   input [2:0] F,
   input [2:0] D
   );

reg [N-1:0] R [7:0];
initial
         begin
               R[0]=8'h00;
               R[1]=8'h19;
               R[2]=8'h25;
               R[3]=8'haa;
               R[4]=8'h50;
               R[5]=8'h22;
               R[6]=8'h43;
               R[7]=8'hf0;
         end

always@(posedge ck)
         if(W)
         case({P1,P0})
               2'b00: R[D] <= R[D] + R[F];
               2'b01: R[D] <= R[D];
               2'b10: R[D] <= R[D] - R[F];
               2'b11: R[D] <= R[F];
         endcase
endmodule
```

```
module ucontrol(
   input ck,
   input XS,
   input I0,
   input I1,
   input reset,
   output reg P0,
   output reg P1,
   output reg W,
   output reg FIN
);

parameter S0 = 2'b00, S1 = 2'b01, SF = 2'b10;

reg [1:0] current_state,next_state;

always @(posedge ck or posedge reset)
        begin
            if(reset)
                current_state <= S0;
            else
                current_state <= next_state;
        end

always @(current_state,I0,I1,XS)
        begin
            P0 = 0;
            P1 = 0;
            FIN = 0;
            W = 0;
            next_state = S0;
            case(current_state)
            S0:
                if(XS) next_state = S1;
            S1:
                begin
                W = 1;
                if(I0)
                    begin
                    P0 = 1;
                    P1 = 1;
                    end
                else if (I1)
                    P1 = 1;
                next_state = SF;
                end
            SF:
                FIN = 1;
            endcase
        end
endmodule
```

```
module calculadora(
    input ck,
    input XS,
    input I1,
    input I0,
    input reset,
    input [2:0] D,
    input [2:0] F,
    output FIN
    );

wire w1,w2,w3;

datos #(.N(8)) ud_calc(.ck(ck),.W(w1),.P0(w2),.P1(w3),.D(D),.F(F));
ucontrol uc_calc(.ck(ck),.reset(reset),.XS(XS),.FIN(FIN),.I0(I0),.I1(I1),
                    .W(w1),.P0(w2),.P1(w3));

endmodule
```

TESTBENCH

```
module calculadora_tb;

            // Inputs
            reg ck;
            reg XS;
            reg I1;
            reg I0;
            reg reset;
            reg [2:0] D;
            reg [2:0] F;

            // Outputs
            wire FIN;

            // Instantiate the Unit Under Test (UUT)
            calculadora uut (
                    .ck(ck),
                    .XS(XS),
                    .I1(I1),
                    .I0(I0),
                    .reset(reset),
                    .D(D),
                    .F(F),
                    .FIN(FIN)
            );
```

```
    always
        begin
        #100;
        ck = ~ck;
        end

    initial begin
        // Initialize Inputs
        ck = 0;
        XS = 0;
        reset = 1;            //obligamos a la u. control a empezar por su estado inicial
        I1 = 0;                // fijo los primeros datos y selecciono la operacion
        I0 = 0;
        D = 1;
        F = 2;

        @(posedge ck);
        reset = 0;
        XS = 1;                //  señal de comienzo

        @(posedge ck);
        XS = 0;

        repeat(3) @(posedge ck);  //damos tiempo a que se haga la primera op.

        XS=1;        // nueva señal de comienzo
        I1=1;         // nuevos datos y nueva operacion
        I0=0;
        D = 5;
        F = 7;

        @(posedge ck);
        XS= 0;

        repeat(3) @(posedge ck);  //damos tiempo a que se haga la segunda op.

        XS=1;          // nueva señal de comienzo
        I1=0;           // nuevos datos y nueva operacion
        I0=1;
        D=4;
        F=5;

        @(posedge ck);
        XS=0;

        repeat(3) @(posedge ck);    //damos tiempo a que se haga la tercera op.
        $finish;
    end

endmodule
```