The **Microelectronics Training Center**

The MTC is an initiative within the INVOMEC division

Industrialization & Training in Microelectronics

Lab-exercise

Lab 4:

Building a basic system

Cluster: Cluster1
Module: Module5b

Target group: Students

Version: 1.0
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http://www.esf-agentschap.be

Introduction

You build the complete system architecture of Micro6 in this module.

Objectives

After completing this module, you should be able to describe structural models in VHDL

Knowledge background

- Basic VHDL knowledge
- Understanding of the system architecture of Micro6 (presented in cluster 0)

Classification

- Level: 2
- Duration: 30 minutes

Input

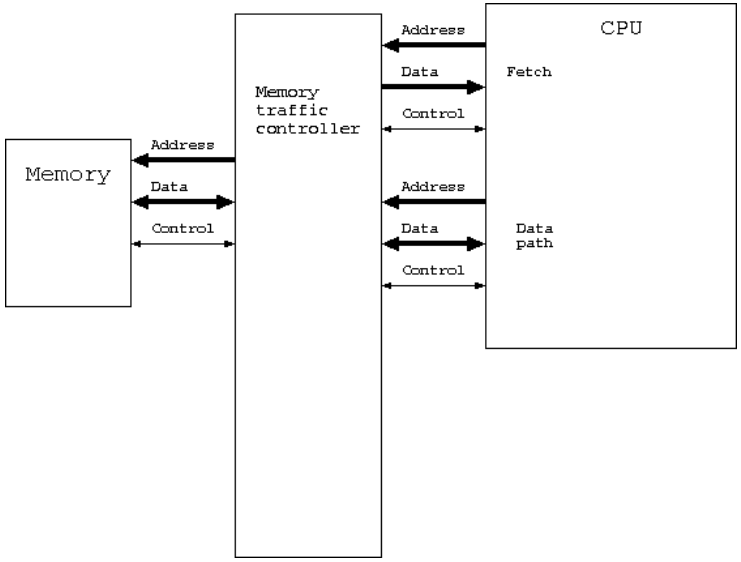
VHDL template

The lab

The system architecture represents the topmost level of Micro6. It is composed of 3 units:

1. The CPU (developed in the previous module);
2. The memory;
3. The memory traffic controller;

How to integrate these units is explained in the previous module.



Complete the VHDL description of the Micro6 system architecture provided in the template file `system.vhd`. The IO unit will not yet be connected in this system. This means that the inputs of the Memory traffic controller that are connected to the IOUnit have to be fixed to zero. Also the direct IO connections from CPU to IOUnit (not shown in above figure) have to be set to zero while the direct connections from IOUnit to CPU have to be left unconnected (also not shown in above figure).
Use compile.do to compile all modules in Modelsim.

In the next module we will verify this system.