The **Microelectronics Training Center**

The MTC is an initiative within the INVOMEC division

Industrialization & Training in Microelectronics

Lab-exercise

Lab 4:

Implement and verify the complete system including a Uart

Cluster: Cluster2
Module: Module6b

Target group: Students

Version: 1.1
Date: 15/02/07
Author: Geert Vanwijnsberghe
Modified by:

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http://www.esf-agentschap.be

Introduction

In this module, you implement your microprocessor on the XUP board and run the simple program developed in module 6a to reverse the characters in a string.

Objectives

After completing this module, you should be able to:

- Implement designs using ISE
- Configure FPGA devices

Knowledge background

- Basic knowledge of an FPGA design flow

Classification

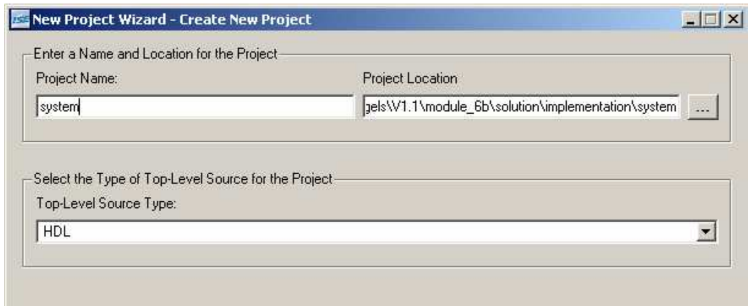
- Level: 2
- Duration: 1 hour

Input

The solution of module6a and the system.ucf (inside the implementation folder) are actually used as input for this module.

The lab

1. Copy the complete input folder to <your_module6b_folder>.
2. Start Xilinx ISE (Project navigator) by clicking on **Xilinx ISE 8.2i** → **Project Navigator** from the **Start** menu.
3. When another project is currently active, close it : **File** → **Close project**
4. Create a new project: **File** → **New Project...**
5. In the **New Project** window, enter a **Project Name** "system" and choose the <your_module6b_folder>/implementation as the **Project Location**.



Enter a Name and Location for the Project

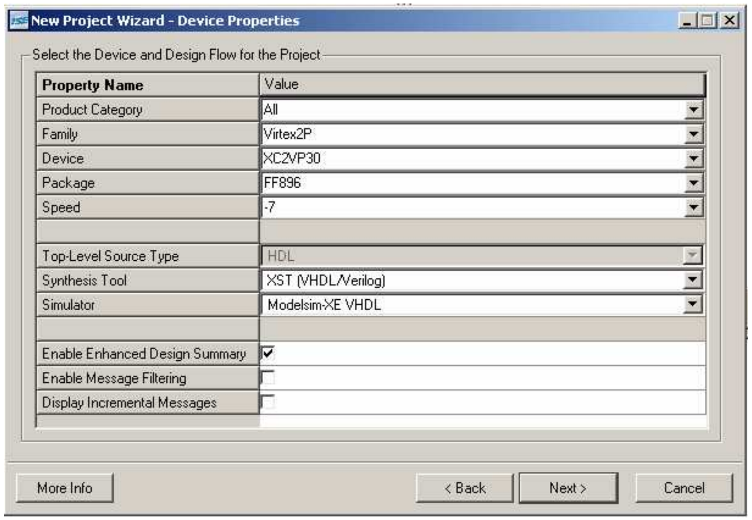
Project Name: system

Project Location: gels\V1.1\module_6b\solution\implementation\system

Select the Type of Top-Level Source for the Project

Top-Level Source Type: HDL

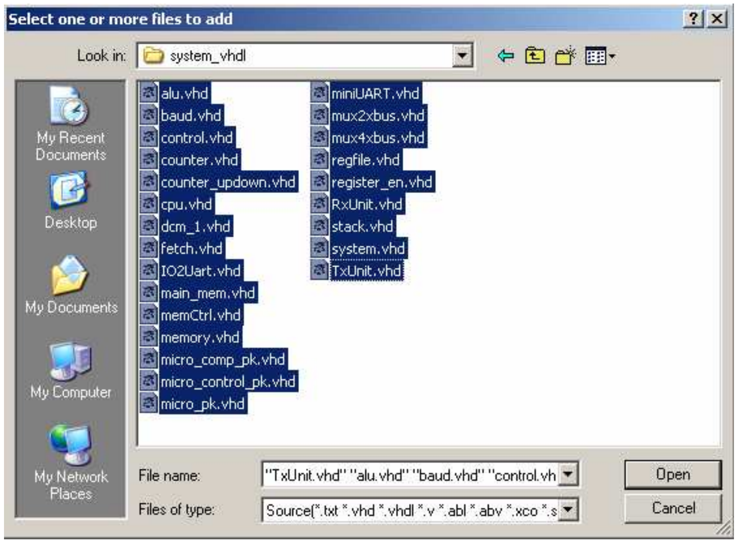
6. Click **Next**. In the next window, **select the Family, Device etc…**for the Project as shown below.



Select the Device and Design Flow for the Project

Property Name	Value
Product Category	All
Family	Virtex2P
Device	XC2VP30
Package	FF896
Speed	-7
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	Modelsim-XE VHDL
Enable Enhanced Design Summary	☑
Enable Message Filtering	☐
Display Incremental Messages	☐

7. Click **Next**. You don't need to create any new sources, so skip this window by clicking **Next** again.
8. In the current window, you **Add Existing Sources**. Press the **Add Source** button. Browse to the directory where the design files are stored (system_hdl) and select all .vhd files.



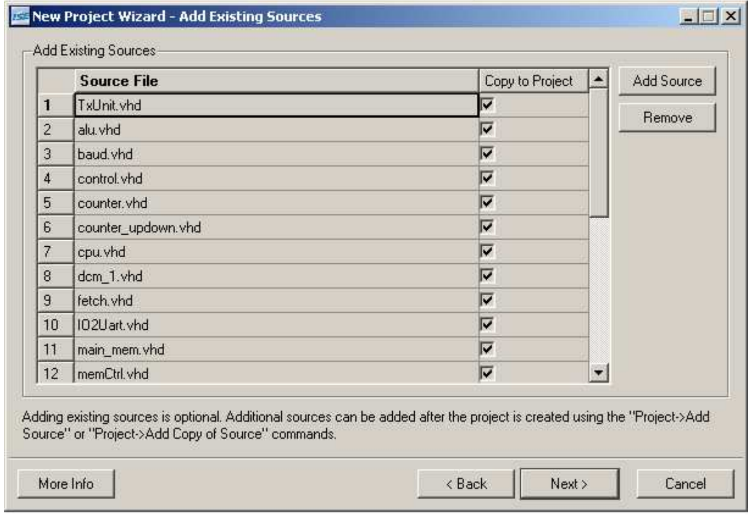
Look in: system_vhdl

alu.vhd
baud.vhd
control.vhd
counter.vhd
counter_updown.vhd
cpu.vhd
dcm_1.vhd
fetch.vhd
IO2Uart.vhd
main_mem.vhd
memCtrl.vhd
memory.vhd
micro_comp_pk.vhd
micro_control_pk.vhd
micro_pk.vhd
miniUART.vhd
mux2xbus.vhd
mux4xbus.vhd
regfile.vhd
register_en.vhd
RxUnit.vhd
stack.vhd
system.vhd
TxUnit.vhd

File name: "TxUnit.vhd" "alu.vhd" "baud.vhd" "control.vh

Files of type: Source(*.txt *.vhd *.vhdl *.v *.abl *.abv *.xco *.s

9. Terminate the Add Existing Sources window by clicking on Open.



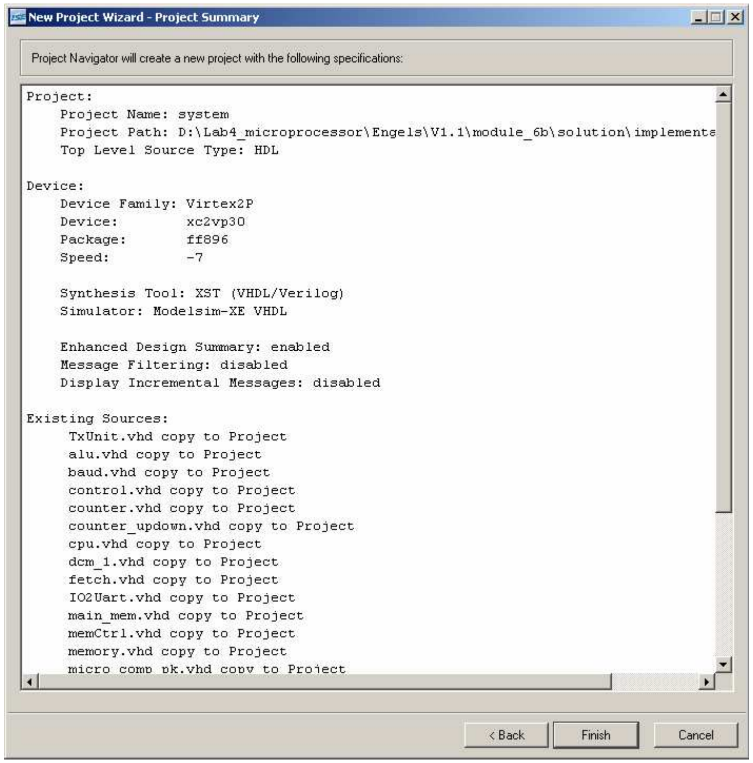
Add Existing Sources

	Source File	Copy to Project
1	TxUnit.vhd	☑
2	alu.vhd	☑
3	baud.vhd	☑
4	control.vhd	☑
5	counter.vhd	☑
6	counter_updown.vhd	☑
7	cpu.vhd	☑
8	dcm_1.vhd	☑
9	fetch.vhd	☑
10	IO2Uart.vhd	☑
11	main_mem.vhd	☑
12	memCtrl.vhd	☑

Adding existing sources is optional. Additional sources can be added after the project is created using the "Project->Add Source" or "Project->Add Copy of Source" commands.

Click **next**.

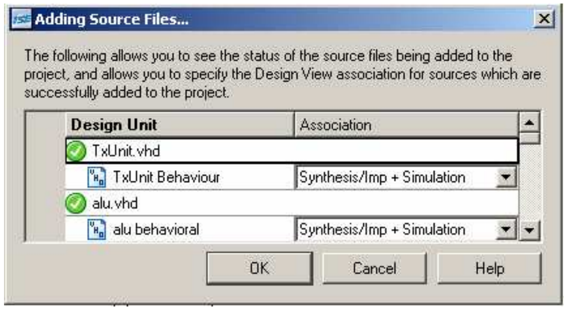
10. Now you get a summary of all the files that are copied to your project. Click **Finish**.



Project Navigator will create a new project with the following specifications:

```
Project:
    Project Name: system
    Project Path: D:\Lab4_microprocessor\Engels\V1.1\module_6b\solution\implementa
    Top Level Source Type: HDL

Device:
    Device Family: Virtex2P
    Device:        xc2vp30
    Package:       ff896
    Speed:         -7

    Synthesis Tool: XST (VHDL/Verilog)
    Simulator: Modelsim-XE VHDL

    Enhanced Design Summary: enabled
    Message Filtering: disabled
    Display Incremental Messages: disabled

Existing Sources:
     TxUnit.vhd copy to Project
     alu.vhd copy to Project
     baud.vhd copy to Project
     control.vhd copy to Project
     counter.vhd copy to Project
     counter_updown.vhd copy to Project
     cpu.vhd copy to Project
     dcm_1.vhd copy to Project
     fetch.vhd copy to Project
     IO2Uart.vhd copy to Project
     main_mem.vhd copy to Project
     memCtrl.vhd copy to Project
     memory.vhd copy to Project
     micro_comp_pk.vhd copy to Project
```

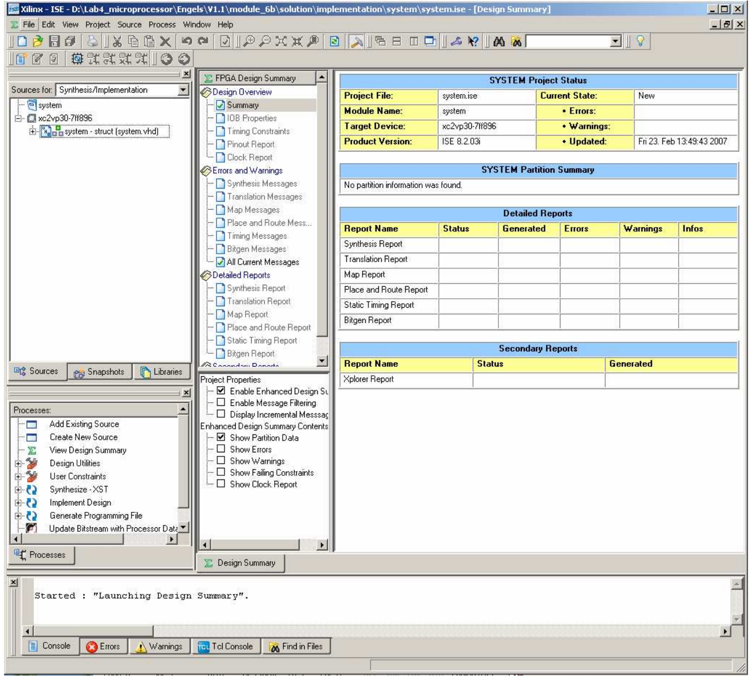
Click **OK**.



The following allows you to see the status of the source files being added to the project, and allows you to specify the Design View association for sources which are successfully added to the project.

Design Unit	Association
TxUnit.vhd	
TxUnit Behaviour	Synthesis/Imp + Simulation
alu.vhd	
alu behavioral	Synthesis/Imp + Simulation

11. You are now back at the design summary**.**



Project Properties
- ☑ Enable Enhanced Design Su
- ☐ Enable Message Filtering
- ☐ Display Incremental Messag

Enhanced Design Summary Contents
- ☑ Show Partition Data
- ☐ Show Errors
- ☐ Show Warnings
- ☐ Show Failing Constraints
- ☐ Show Clock Report

SYSTEM Project Status

Project File:	system.ise	**Current State:**	New
Module Name:	system	**• Errors:**	
Target Device:	xc2vp30-7ff896	**• Warnings:**	
Product Version:	ISE 8.2.03i	**• Updated:**	Fri 23. Feb 13:49:43 2007

SYSTEM Partition Summary

No partition information was found.

Detailed Reports

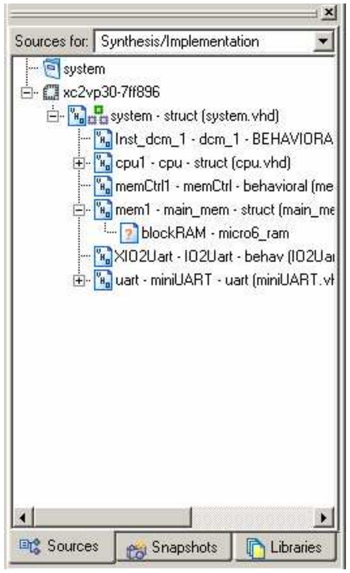
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report					
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

Secondary Reports

Report Name	Status	Generated
Xplorer Report		

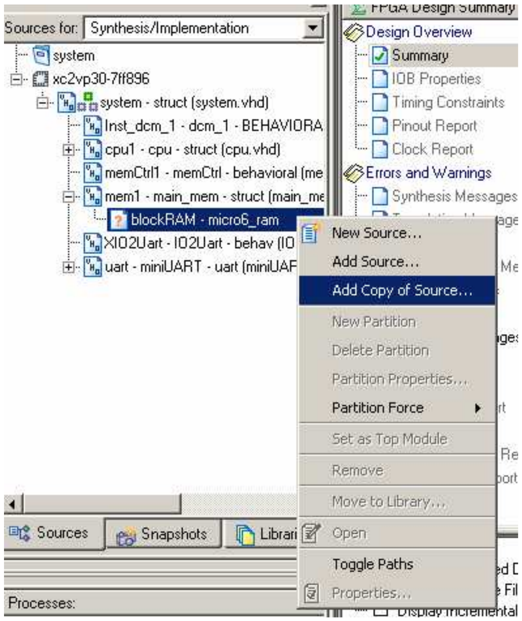
```
Started : "Launching Design Summary".
```

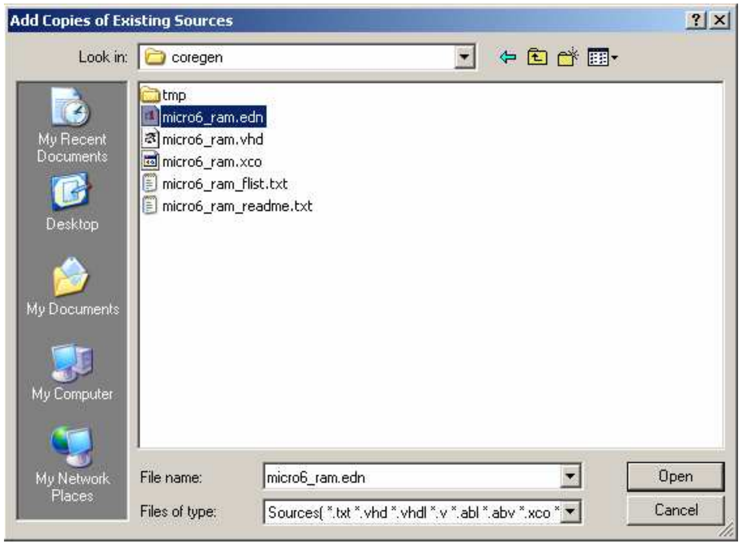
12. In the sources window you can expand system (hit the + sign before system-struct). If you also expand mem1 you will see that there is still a ? before the internal blockRAM.


Sources for: Synthesis/Implementation

system
xc2vp30-7ff896
system - struct (system.vhd)
Inst_dcm_1 - dcm_1 - BEHAVIORA
cpu1 - cpu - struct (cpu.vhd)
memCtrl1 - memCtrl - behavioral (me
mem1 - main_mem - struct (main_me
blockRAM - micro6_ram
XIO2Uart - IO2Uart - behav (IO2Ua
uart - miniUART - uart (miniUART.vh
Sources
Snapshots
Libraries

13. Add the edif description of the blockRAM that was created in the previous module 6a as shown in the next figures. At the end you will see that the question mark before the blockRAM has been replaced by an edif icon.

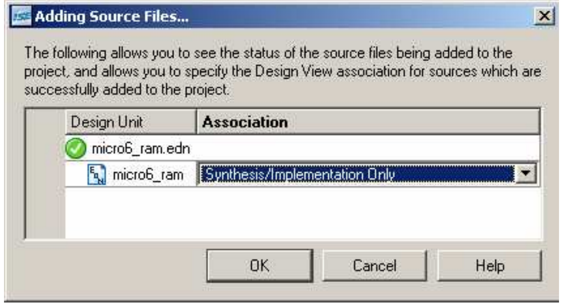

Sources for: Synthesis/Implementation


Add Copies of Existing Sources

Look in: coregen

File name: micro6_ram.edn

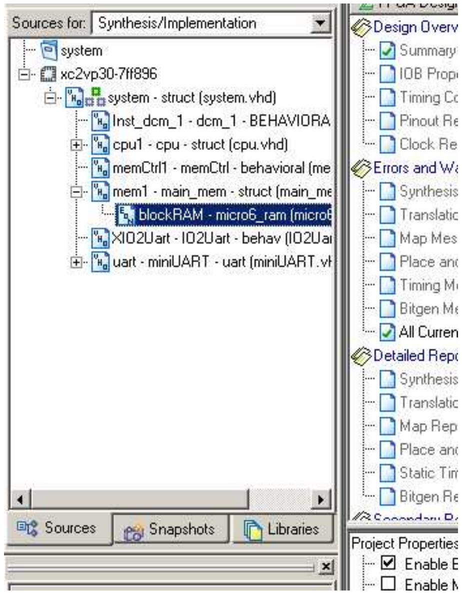
Files of type: Sources(*.txt *.vhd *.vhdl *.v *.abl *.abv *.xco *



Adding Source Files...

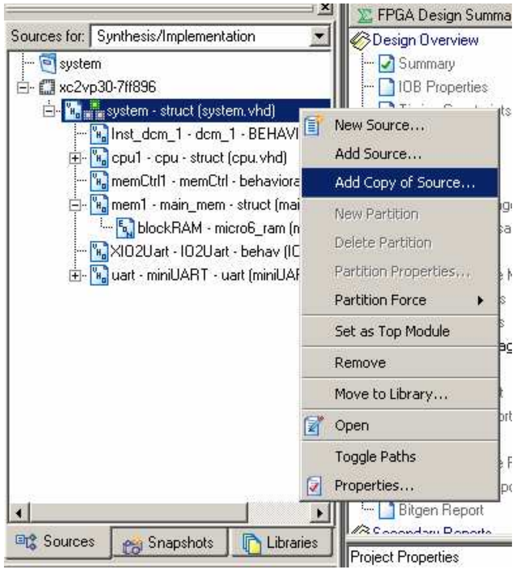
The following allows you to see the status of the source files being added to the project, and allows you to specify the Design View association for sources which are successfully added to the project.

Design Unit	Association
✓ micro6_ram.edn	
micro6_ram	Synthesis/Implementation Only



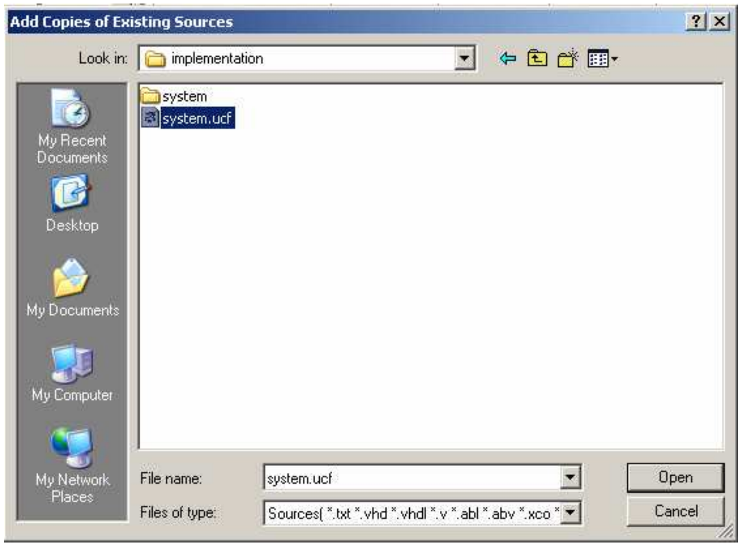
Sources for: Synthesis/Implementation

14. Before we can start the synthesis and implementation of the design into the FPGA we still have to specify the constraints. In this design the only constraints that we will apply are: mapping of the IO pins of system to the IO pads of the FPGA and the frequency of the clock. These constraints were written in system.ucf. Add this constraints file to system as follows:



Sources for: Synthesis/Implementation

15. Browse to the implementation folder and choose `system.ucf` and click **Open**.



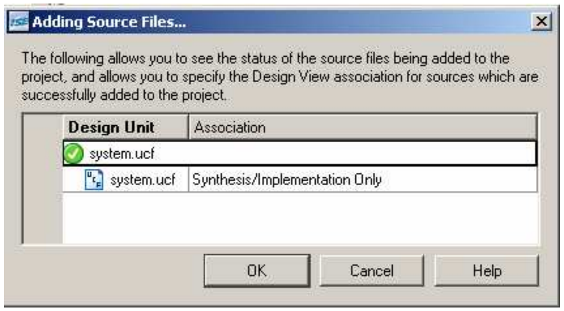
Add Copies of Existing Sources

Look in: implementation

system
system.ucf

File name: system.ucf

Files of type: Sources(*.txt *.vhd *.vhdl *.v *.abl *.abv *.xco *



Adding Source Files...

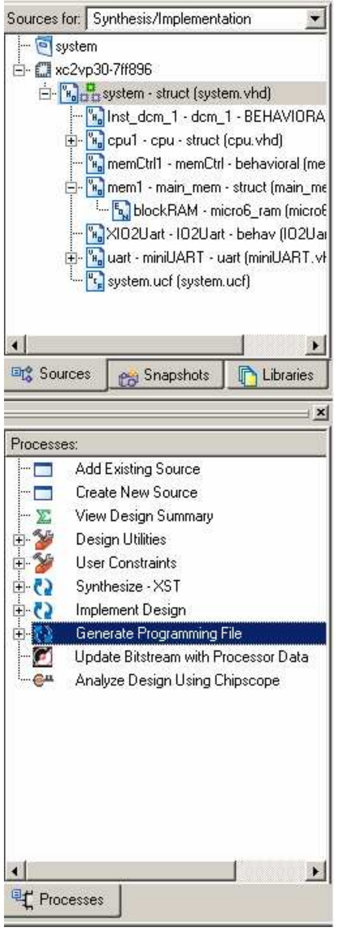
The following allows you to see the status of the source files being added to the project, and allows you to specify the Design View association for sources which are successfully added to the project.

Design Unit	Association
✓ system.ucf	
system.ucf	Synthesis/Implementation Only

Hit **OK** and system.ucf will be added in the Sources window.

16. Now you are ready to implement your design. Choose the top level of your design in the **Sources** pane. In this case, it is `system-struct (system.vhd)`. Double-click

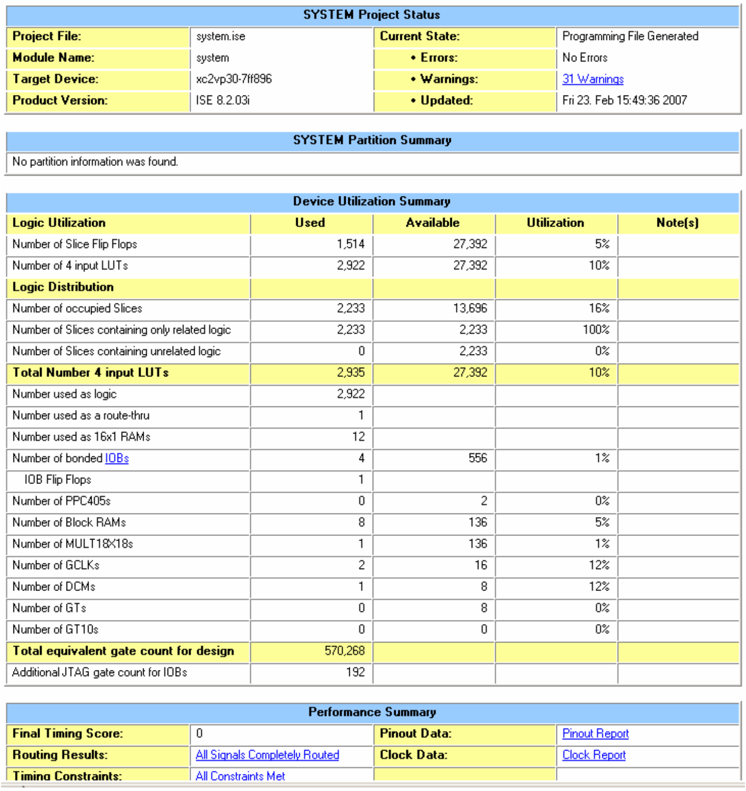
Generate Programming File in the **Processes** pane.



Sources for: Synthesis/Implementation

system
xc2vp30-7ff896
system - struct (system.vhd)
Inst_dcm_1 - dcm_1 - BEHAVIORA
cpu1 - cpu - struct (cpu.vhd)
memCtrl1 - memCtrl - behavioral (me
mem1 - main_mem - struct (main_me
blockRAM - micro6_ram (micro6
XIO2Uart - IO2Uart - behav (IO2Ua
uart - miniUART - uart (miniUART.vh
system.ucf (system.ucf)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Update Bitstream with Processor Data
Analyze Design Using Chipscope
Processes

17. Xilinx ISE synthesizes the design and performs placement and routing and then generates the programming file. This procedure takes 3 to 5 minutes.



SYSTEM Project Status			
Project File:	system.ise	**Current State:**	Programming File Generated
Module Name:	system	**• Errors:**	No Errors
Target Device:	xc2vp30-7ff896	**• Warnings:**	31 Warnings
Product Version:	ISE 8.2.03i	**• Updated:**	Fri 23. Feb 15:49:36 2007

SYSTEM Partition Summary
No partition information was found.

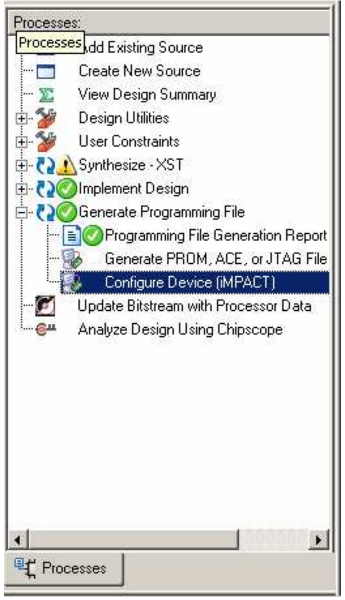
Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	1,514	27,392	5%	
Number of 4 input LUTs	2,922	27,392	10%	
Logic Distribution				
Number of occupied Slices	2,233	13,696	16%	
Number of Slices containing only related logic	2,233	2,233	100%	
Number of Slices containing unrelated logic	0	2,233	0%	
Total Number 4 input LUTs	2,935	27,392	10%	
Number used as logic	2,922			
Number used as a route-thru	1			
Number used as 16x1 RAMs	12			
Number of bonded IOBs	4	556	1%	
IOB Flip Flops	1			
Number of PPC405s	0	2	0%	
Number of Block RAMs	8	136	5%	
Number of MULT18X18s	1	136	1%	
Number of GCLKs	2	16	12%	
Number of DCMs	1	8	12%	
Number of GTs	0	8	0%	
Number of GT10s	0	0	0%	
Total equivalent gate count for design	570,268			
Additional JTAG gate count for IOBs	192			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

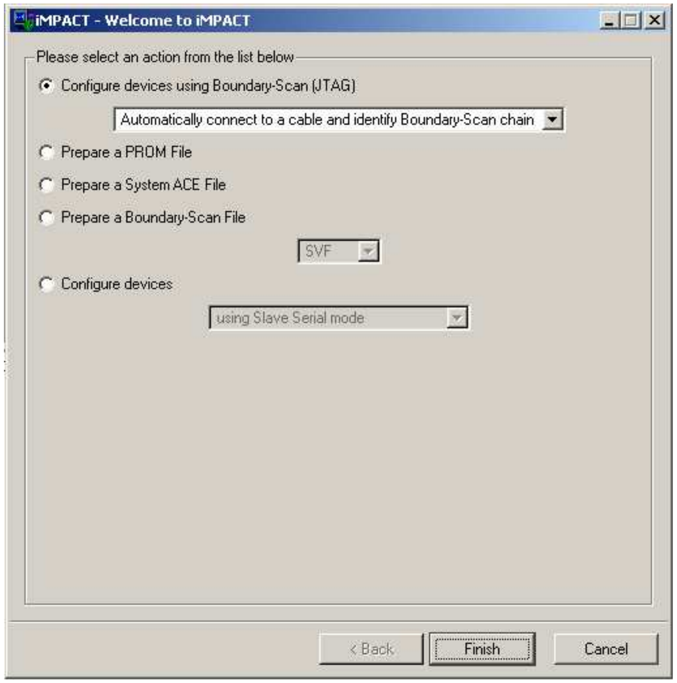
Have a look at the design summary. There should be no errors, the 4 IOs have to be bonded, all the signals have to be routed and all constraints should be met.

18. When ready, connect the USB cable and the serial cable of the XUP board with your PC. Now switch on the power of the board. You should get a message that an USB device has been detected.

19. Expand the Generate Programming File in the Processes pane.

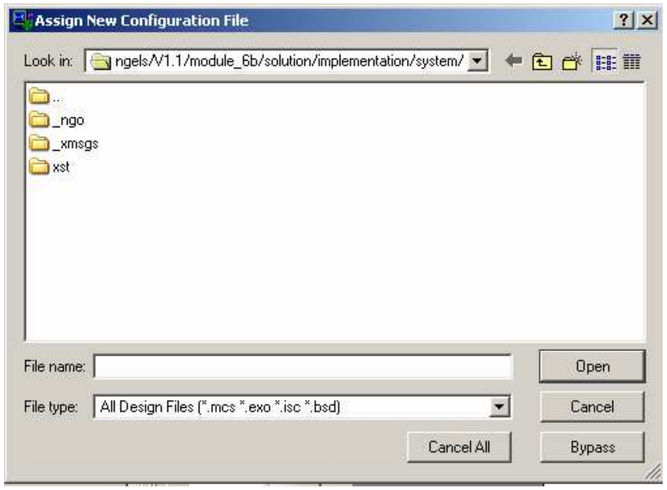

Processes:
Processes
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Update Bitstream with Processor Data
Analyze Design Using Chipscope
Processes

20. Double-click the **Configure Device (IMPACT)** process in the Processes pane.
21. IMPACT starts and the **Configure Devices** window is displayed. Click **Next** without changing the default settings.

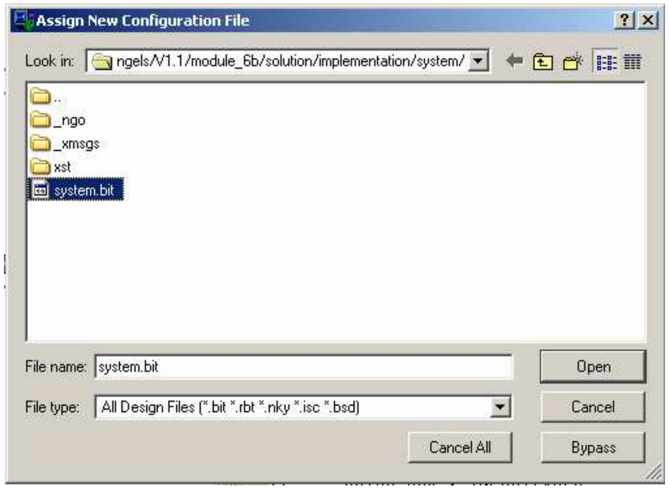

iMPACT - Welcome to iMPACT
Please select an action from the list below
● Configure devices using Boundary-Scan (JTAG)
Automatically connect to a cable and identify Boundary-Scan chain
○ Prepare a PROM File
○ Prepare a System ACE File
○ Prepare a Boundary-Scan File
SVF
○ Configure devices
using Slave Serial mode
< Back
Finish
Cancel

Click **Finish**.

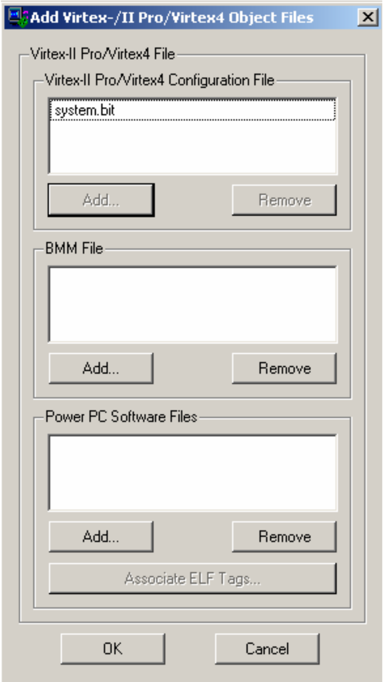
22. For the first 2 devices, click **Bypass** when the **Assign New Configuration File** window is displayed.


Assign New Configuration File
Look in: ngels/V1.1/module_6b/solution/implementation/system/
..
_ngo
_xmsgs
xst
File name:
File type: All Design Files (*.mcs *.exo *.isc *.bsd)
Open
Cancel
Cancel All
Bypass

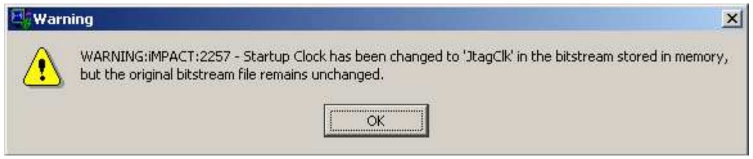
23. The third device is the target FPGA. Choose the file `system.bit` and click **Open**.


Assign New Configuration File
Look in: ngels/V1.1/module_6b/solution/implementation/system/
..
_ngo
_xmsgs
xst
system.bit
File name: system.bit
File type: All Design Files (*.bit *.rbt *.nky *.isc *.bsd)
Open
Cancel
Cancel All
Bypass

24. **Add Virtex-II Pro/Virtex 4 Object Files** window is displayed. Click **OK**.

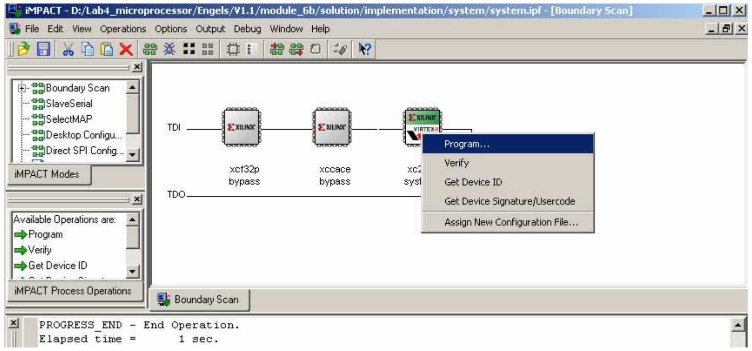


25. Accept the following Warning message.



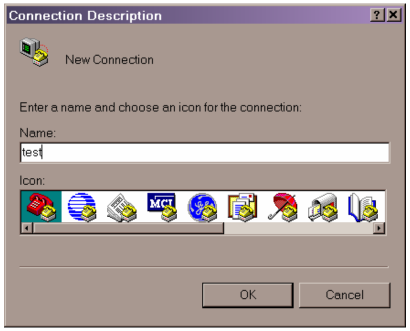
WARNING:iMPACT:2257 - Startup Clock has been changed to 'JtagClk' in the bitstream stored in memory, but the original bitstream file remains unchanged.

26. Right-click the FPGA device and select **Program** to start the configuration.



```
PROGRESS_END - End Operation.
Elapsed time =      1 sec.
```

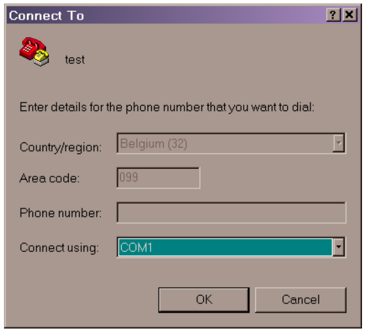
27. Accept the default settings in the **Program Options** window.
    Now you get a programmed successfully message.
28. Start **HyperTerminal** from the Start Menu by choosing **Programs** → **Accessories** → **Communications** → **HyperTerminal**.
29. In the **Connection Description** window, enter `test` as the **Name** of the connection and click **OK**.



Enter a name and choose an icon for the connection:

Name: test

30. Click **OK** to accept the default setting in the **Connect To** window.



Connect To

test

Enter details for the phone number that you want to dial:

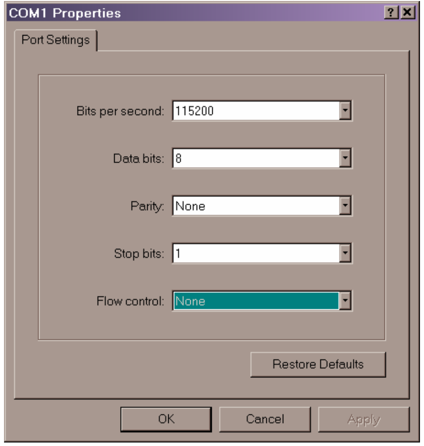
Country/region: Belgium (32)

Area code: 099

Phone number:

Connect using: COM1

31. In the **COM1 Properties** window do the following changes:
Bits per second: 115200
Flow Control: None
Leave the remaining settings unchanged and click **OK**.



COM1 Properties

Port Settings

Bits per second: 115200

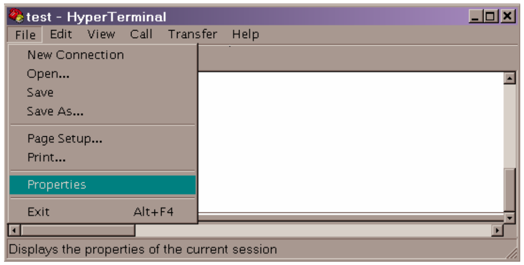
Data bits: 8

Parity: None

Stop bits: 1

Flow control: None

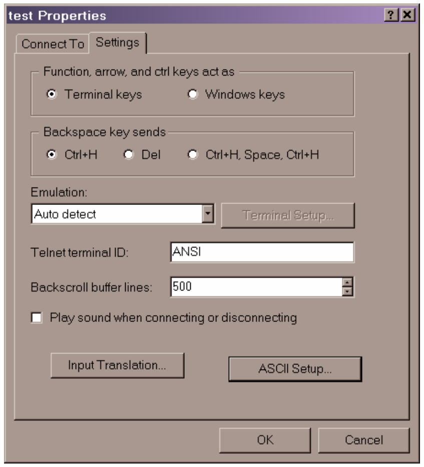
32. Click on File → Properties in the main window of HyperTerminal.



test - HyperTerminal

Displays the properties of the current session

33. Choose the **Settings** tab in the **test Properties** window. Press **ASCII Setup** button and check **Echo typed characters locally**. Click **OK**. Dismiss the **Properties** window by clicking **OK**.



test Properties

Connect To | Settings

Function, arrow, and ctrl keys act as
● Terminal keys ○ Windows keys

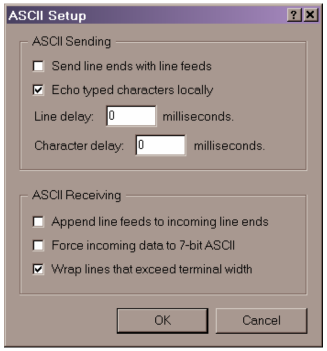
Backspace key sends
● Ctrl+H ○ Del ○ Ctrl+H, Space, Ctrl+H

Emulation: Auto detect

Telnet terminal ID: ANSI

Backscroll buffer lines: 500

☐ Play sound when connecting or disconnecting



ASCII Setup

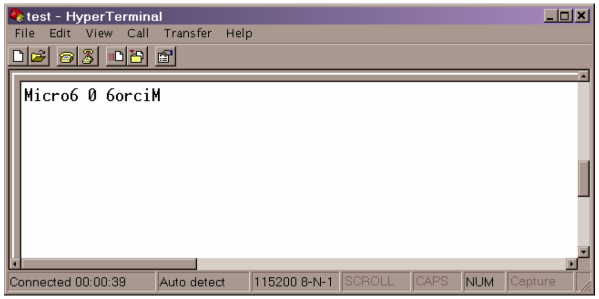
ASCII Sending

- ☐ Send line ends with line feeds
- ☑ Echo typed characters locally
- Line delay: 0 milliseconds.
- Character delay: 0 milliseconds.

ASCII Receiving

- ☐ Append line feeds to incoming line ends
- ☐ Force incoming data to 7-bit ASCII
- ☑ Wrap lines that exceed terminal width

34. A connection with Micro6 is established. The program that Micro6 runs accepts a string of characters terminated by ‘0’. When ‘0’ is received, Micro6 echoes the string you have entered after reversing the order of its characters.



```
Micro6 0 6orciM
```

Connected 00:00:39 | Auto detect | 115200 8-N-1 | SCROLL | CAPS | NUM | Capture

Congratulations!!!

35. You can restart the program by pressing the **SW2** switch on the board.