



Informática: Computer Science. Computing.

Oxford Spanish Dictionary

Computers are also **"Computing"**

Digital Electronic Computers are also **"Computing"**

El **Hardware** también es **Informática**

Informática

Software
Redes de computadores
Computadores
Sistemas digitales
Circuitos digitales
Circuitos analógicos
Teoría de circuitos
Electrónica
Física

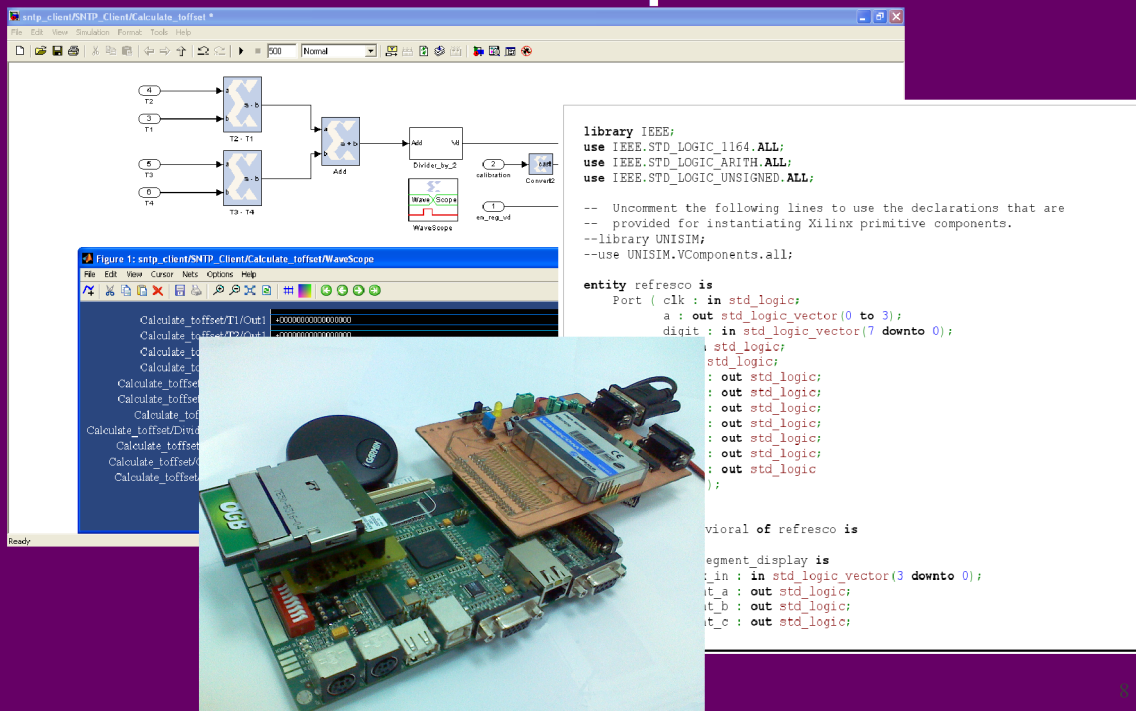


Hacer **hardware** es parecido a hacer **software**

```
always @(a, b, c)
  if(a == 1)
    if(b == 1 || c == 1)
      f = 1;
    else
      f = 0;
  else
    if(b == 1 && c == 1)
      f = 1;
    else
      f = 0;
```

```
while (a | b | c)
  if(a == 1)
    if(b == 1 || c == 1)
      f = 1;
    else
      f = 0;
  else
    if(b == 1 && c == 1)
      f = 1;
    else
      f = 0;
```

Sistemas empotrados



The image displays a screenshot of a hardware design tool interface. At the top, a logic diagram shows inputs a, b, c, d, T2, T1, T3, and T4 connected to various logic blocks including multipliers (x2, x4), an adder, a divider (Divide_by_2), and a counter (Count). Below the diagram is a waveform viewer showing signals for Calculate_offset/T1/Out, Calculate_offset/T2/Out, Calculate_offset/T3, Calculate_offset/T4, Calculate_offset/Divide_by_2, Calculate_offset/Count, and Calculate_offset/Out. To the right, a Verilog code editor shows the following code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

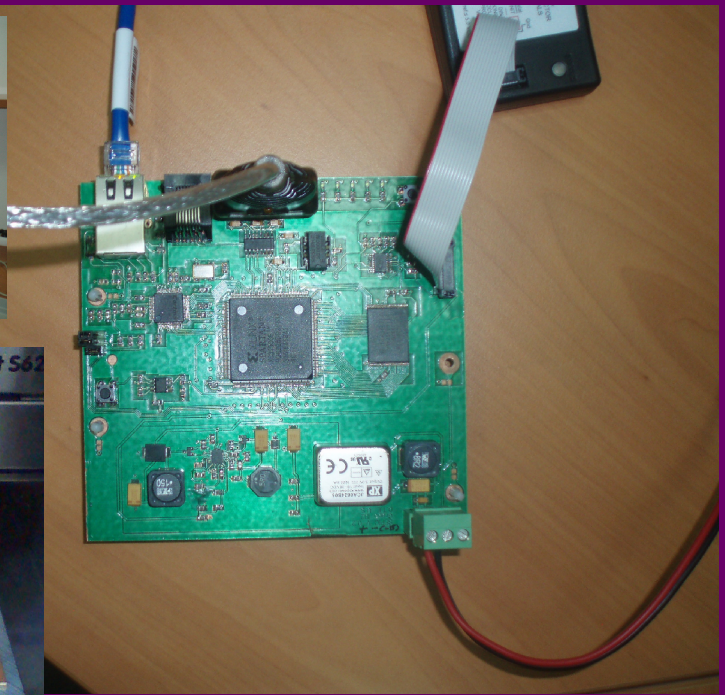
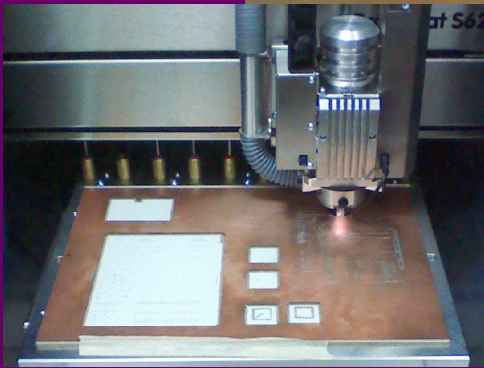
-- Uncomment the following lines to use the declarations that are
-- provided for instantiating Xilinx primitive components.
--library UNISIM;
--use UNISIM.VComponents.all;

entity refresco is
  Port ( clk : in std_logic;
        a : out std_logic_vector(0 to 3);
        digit : in std_logic_vector(7 downto 0);
        : std_logic;
        : out std_logic;
        : out std_logic;
        : out std_logic;
        : out std_logic;
        : out std_logic;
        : out std_logic;
        : out std_logic;
        : out std_logic;
        );

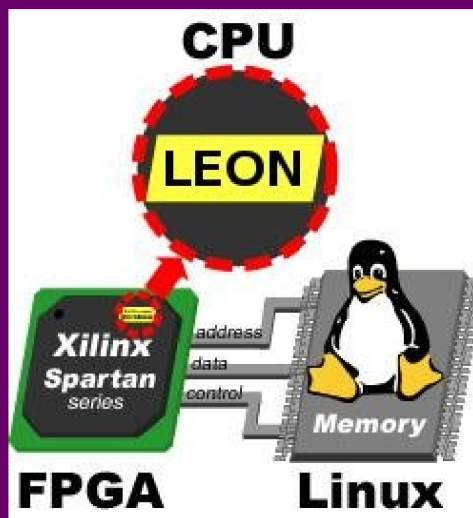
behavioral of refresco is

segment_display is
  _in : in std_logic_vector(3 downto 0);
  _t_a : out std_logic;
  _t_b : out std_logic;
  _t_c : out std_logic;
```


Sistemas empotrados

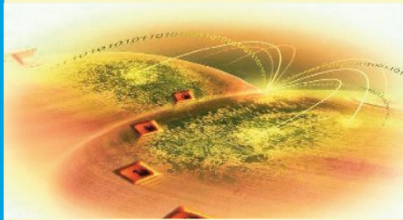


Sistemas empotrados





Máster Universitario en Ingeniería de Computadores y Redes



Desarrollo Curricular

1^{er} Cuatrimestre (30 ECTS)

Obligatorios

- Diseño Avanzado de Redes
- Diseño y Aplicaciones de Procesadores Avanzados
- Diseño con Microcontroladores

Optativos

- Diseño de Interfaces Hardware para PC
- Gestión e Innovación, la Calidad y el Conocimiento en las Empresas y Organizaciones
- Procesado de Bioseñales en Sistemas Empotrados y Comunicaciones
- Compatibilidad Electromagnética

2^o Cuatrimestre (30 ECTS)

Obligatorio: Trabajo Fin de Máster

Por especialidad (24 ECTS)

- +Sistemas Empotrados
 - Diseño de Sistemas Empotrados
 - Aplicaciones de Sistemas Empotrados
- +Redes y Sistemas Distribuidos
 - Sistemas Distribuidos
 - Redes

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