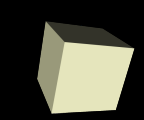
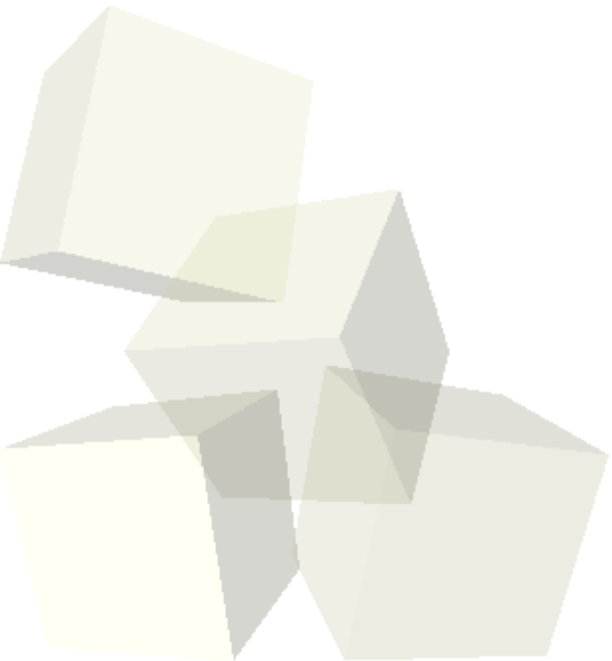


Introducción a lowRISC

Manuel J. Bellido Díaz

Febrero de 2017



Introducción a lowRISC

- www.lowrisc.org :
  - *"A fully open-sourced, Linux-capable, System-on-a-Chip"*
- Completamente abierto: Basado en la arquitectura **RISC V 64 bits**
  - Otras características: seguridad, flexiblidad, ...
- Hasta ahora: varios tutoriales
  - Versión "thetered", "unthetered" y con soporte para debug
- Quienes fundan el proyecto:
  - Universidad de cambridge: provienen de proyecto Raspberri Py
- Presentación de lowRISC en ORCONF2016 (octubre 2016):
  - http://orconf.org/2016/
  - https://youtu.be/52QucTks68Y

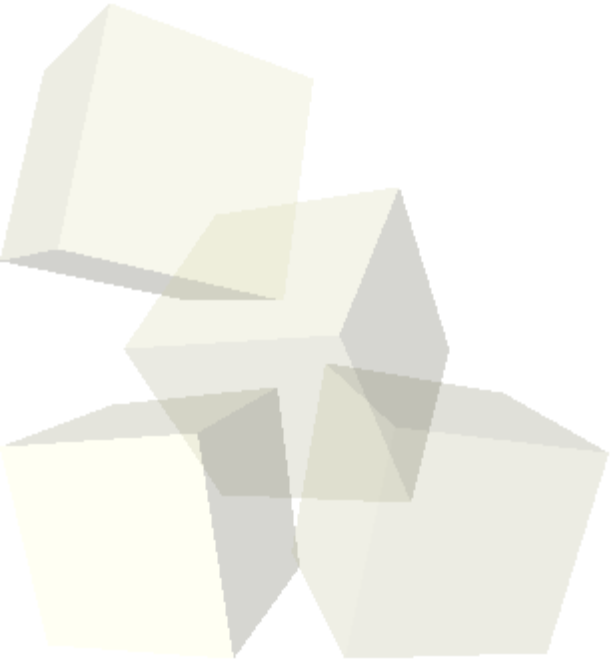
Introducción a RISC-V (Risc five)

"RISC-V (pronounced "risk-five") is a new instruction set architecture (ISA) that was originally designed to support computer architecture research and education and is now set to become a standard open architecture for industry implementations under the governance of the RISC-V Foundation.

RISC-V was originally developed in the Computer Science Division of the EECS Department at the University of California, Berkeley."

- *¿Porque desarrollar un nuevo ISA, porque abierto y cual es el objetivo a medio plazo?*
  - En lo que sigue emplearemos transparencias de los workshops de RISC-V: http://riscv.org/workshops/

RESUMEN DE LAS PRESENTACIONES DE INTRODUCCIÓN A RISC-V EN LOS WORKSHOPS Y EVENTOS PRESENTADOS



ISAs don't matter

Most of the performance and energy running software on a computer is due to:

- Algorithms
- Application code
- Compiler
- OS/Runtimes
- ISA (Instruction Set Architecture)
- Microarchitecture (core + memory hierarchy)
- Circuit design
- Physical design
- Fabrication process

In a *system*, there's also displays, radios, DC/DC convertors, sensors, actuators, …

ISAs do matter

- Most important interface in computer system
- Large cost to port and tune all ISA-dependent parts of a modern software stack
- Large cost to recompile/port/QA all supposedly ISA-independent parts of stack
- Proprietary closed-source, don't have code
- Bit rot, lose ability to compile own source code
- Lost your own source code

- Most of the cost of developing a new chip is developing software for it
- Most big new chips have several ISAs…

So…

If choice of ISA doesn't have much impact on system energy/ performance,
and it costs a lot to use different ones

Why isn't there a free, open standard ISA that everyone can use for everything?

Open Software/Standards Work!

Field	*Standard*	*Free, Open Impl.*	*Proprietary Impl.*
Networking	Ethernet, TCP/IP	Many	Many
OS	Posix	Linux, FreeBSD	M/S Windows
Compilers	C	gcc, LLVM	Intel icc, ARMcc
Databases	SQL	MySQL, PostgresSQL	Oracle 12C, M/S DB2
Graphics	OpenGL	Mesa3D	M/S DirectX
Architecture	--	--	x86, ARM

- Why not successful free & open standards and free & open implementations, like other fields?

ISAs Should Be Free and Open

- ISAs proprietary for historical business reasons, no good reason for the lack of free, open ISAs:
- Not an error of omission by ISA owners
- Nor because owners do most software development
- Nor are most popular ISAs, wonderful ISAs
- Nor are companies great stewards of an ISA
- Nor can only owners verify ISA compatibility
- Not as if buying ISA protects you from patent lawsuits
- Finally, proprietary ISAs are not guaranteed to last, and many actually disappear

RISC-V Background

- In 2010, after many years and many projects using MIPS, SPARC, and x86 as basis of research, time to look at ISA for next set of projects
- Obvious choices: x86 and ARM
- x86 impossible – too complex, IP issues
  - 1300 instructions, x86 ISA manual 2900 pages, instruction length 1 to 15 bytes, ...
- ARM mostly impossible - baroque, IP issues
  - 400 instructions, ARMv7 ISA manual 2700 pages
- So we started "3-month project" in summer 2010 to develop our own clean-slate ISA
- Four years later, we released frozen base user spec
  - But also many tape outs and several research publications

What is RISC-V?

- A new free and open ISA developed at UC Berkeley starting in 2010 (ParLab and ASPIRE)
  - Free as in “beer”, and free as in “speech”
- Designed for
  - research
  - education
  - commercial use
- Not just a free ISA, we also think it’s a good ISA

What's Different about RISC-V?

- *Simple*
  - Far smaller than other commercial ISAs
- *Clean-slate design*
  - Clear separation between user and privileged ISA
  - Avoids µarchitecture or technology-dependent features
- A *modular* ISA
  - Small standard base ISA
  - Multiple standard extensions
- Designed for *extensibility/specialization*
  - Variable-length instruction encoding
  - Vast opcode space available for instruction-set extensions
- *Stable*
  - Base and standard extensions are frozen
  - Additions via optional extensions, not new versions

RISC-V is NOT an Open-Source Processor

- RISC-V is an ISA *specification*
- Want to encourage both open-source and proprietary implementations of the RISC-V ISA specification
- Most of cost of hardware design is software, so make sure software can be reused across many chip designs
- Expand to have open specifications for whole platforms, including I/O and accelerators

Frozen RISC-V Base + Standard Extensions

- ~~Three~~ Four base integer ISAs
  - RV32E, RV32I, RV64I, RV128I
  - RV32E is 16-register subset of RV32I
  - Only <50 hardware instructions needed
- Standard extensions
  - M: Integer multiply/divide
  - A: Atomic memory operations (AMOs + LR/SC)
  - F: Single-precision floating-point
  - D: Double-precision floating-point
  - G = IMAFD, "General-purpose" ISA
  - Q: Quad-precision floating-point
- All the above are a fairly standard RISC encoding in a fixed 32-bit instruction format
- Above user-level ISA components frozen in 2014
  - Supported forever after

ARMv8 ISA vs. RISC-V ISA

Category	ARMv8	RISC-V	ARM/RISC
Year announced	2011	2011	--
Address sizes	32 / 64	32 / 64 / 128	--
Instruction sizes	32	16† / 32	--
Relative code size	1	0.8†	--
Instruction formats	53	6 / 12†	4X-8X
Data addressing modes	8	1	8X
Instructions	1070	177†	6X
Min number instructions to run Linux, gcc, LLVM	359	47	8X
Backend gcc compiler size	47K LOC	10K LOC	5X
Backend LLVM compiler size	22K LOC	10K LOC	2X
ISA manual size	5428 pages	163 pages	33X

MIPS manual 700 pages
80x86 manual 2900 pages

†With optional Compressed RISC-V ISA extension

RISC-V "Green Card"

RV32I / RV64I / RV128I + C, M, A, F, D,& Q

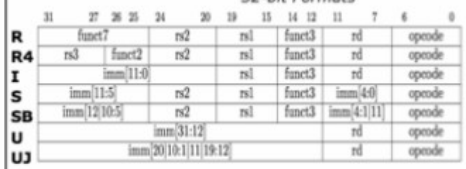
RVI Base Instructions: RV32I, RV64I, and RV128I

Category	Name	Fmt	RV32I Base	+RV64	+RV128
Loads	Load Byte	I	LB rd,rs1,imm		
	Load Halfword	I	LH rd,rs1,imm		
	Load Word	I	LW rd,rs1,imm	LD rd,rs1,imm	LQ rd,rs2,imm
	Load Byte Unsigned	I	LBU rd,rs1,imm		
	Load Half Unsigned	I	LHU rd,rs1,imm	LWU rd,rs1,imm	LDU rd,rs1,imm
Stores	Store Byte	S	SB rs1,rs2,imm		
	Store Halfword	S	SH rs1,rs2,imm		
	Store Word	S	SW rs1,rs2,imm	SD rs1,rs2,imm	SQ rs1,rs2,imm
Arithmetic	ADD	R	ADD rd,rs1,rs2	ADDW rd,rs1,rs2	ADDD rd,rs1,rs2
	ADD Immediate	I	ADDI rd,rs1,imm	ADDIW rd,rs1,imm	ADDID rd,rs1,imm
	SUBtract	R	SUB rd,rs1,rs2	SUBW rd,rs1,rs2	SUBD rd,rs1,rs2
	Load Upper Imm	U	LUI rd,imm		
	Add Upper Imm to PC	U	AUIPC rd,imm		
Shifts	Shift Left	R	SLL rd,rs1,rs2	SLLW rd,rs1,rs2	SLLD rd,rs1,rs2
	Shift Left Immediate	I	SLLI rd,rs1,shamt	SLLIW rd,rs1,shamt	SLLID rd,rs1,shamt
	Shift Right	R	SRL rd,rs1,rs2	SRLW rd,rs1,rs2	SRLD rd,rs1,rs2
	Shift Right Immediate	I	SRLI rd,rs1,shamt	SRLIW rd,rs1,shamt	SRLID rd,rs1,shamt
	Shift Right Arithmetic	R	SRA rd,rs1,rs2	SRAW rd,rs1,rs2	SRAD rd,rs1,rs2
	Shift Right Arith Imm	I	SRAI rd,rs1,shamt	SRAIW rd,rs1,shamt	SRAID rd,rs1,shamt
Logical	XOR	R	XOR rd,rs1,rs2		
	XOR Immediate	I	XORI rd,rs1,imm		
	OR	R	OR rd,rs1,rs2		
	OR Immediate	I	ORI rd,rs1,imm		
	AND	R	AND rd,rs1,rs2		
	AND Immediate	I	ANDI rd,rs1,imm		
Compare	Set <	R	SLT rd,rs1,rs2		
	Set < Immediate	I	SLTI rd,rs1,imm		
	Set < Unsigned	R	SLTU rd,rs1,rs2		
	Set < Unsigned Imm	I	SLTIU rd,rs1,imm		
Branches	Branch =	SB	BEQ rs1,rs2,imm		
	Branch ≠	SB	BNE rs1,rs2,imm		
	Branch <	SB	BLT rs1,rs2,imm		
	Branch ≥	SB	BGE rs1,rs2,imm		
	Branch < Unsigned	SB	BLTU rs1,rs2,imm		
	Branch ≥ Unsigned	SB	BGEU rs1,rs2,imm		
Jump & Link	J&L	UJ	JAL rd,imm		
	Jump & Link Register	UJ	JALR rd,rs1,imm		
Synch	Synch threads	I	FENCE		
	Synch Instr & Data	I	FENCE.I		
System	System CALL	I	SCALL		
	System BREAK	I	SBREAK		
Counters	ReaD CYCLE	I	RDCYCLE rd		
	ReaD CYCLE upper Half	I	RDCYCLEH rd		
	ReaD TIME	I	RDTIME rd		
	ReaD TIME upper Half	I	RDTIMEH rd		
	ReaD INSTR RETired	I	RDINSTRET rd		
	ReaD INSTR upper Half	I	RDINSTRETH rd		

RVC Compressed Instruction Extension

Category	Name	Fmt	RVC	RVI equivalent
Loads	Load Word	CL	C.LW rd',rs1',imm	LW rd',rs1',imm*4
	Load Word SP	CI	C.LWSP rd,imm	LW rd,sp,imm*4
	Load Double	CL	C.LD rd',rs1',imm	LD rd',rs1',imm*8
	Load Double SP	CI	C.LDSP rd,imm	LD rd,sp,imm*8
	Load Quad	CL	C.LQ rd',rs1',imm	LQ rd',rs1',imm*16
	Load Quad SP	CI	C.LQSP rd,imm	LQ rd,sp,imm*16
Stores	Store Word	CS	C.SW rs1',rs2',imm	SW rs1',rs2',imm*4
	Store Word SP	CSS	C.SWSP rs2,imm	SW rs2,sp,imm*4
	Store Double	CS	C.SD rs1',rs2',imm	SD rs1',rs2',imm*8
	Store Double SP	CSS	C.SDSP rs2,imm	SD rs2,sp,imm*8
	Store Quad	CS	C.SQ rs1',rs2',imm	SQ rs1',rs2',imm*16
	Store Quad SP	CSS	C.SQSP rs2,imm	SQ rs2,sp,imm*16
Arithmetic	ADD	CR	C.ADD rd,rs1	ADD rd,rd,imm
	ADD Word	CR	C.ADDW rd,rs1	ADDW rd,rd,imm
	ADD Immediate	CI	C.ADDI rd,imm	ADDI rd,rd,imm
	ADD Word Imm	CI	C.ADDIW rd,imm	ADDIW rd,rd,imm
	ADD Imm * 4	CI	C.ADDI4 rd,imm	ADDI rd,rd,imm*4
	Load Immediate	CI	C.LI rd,imm	ADDI rd,x0,imm
	Load Upper Imm	CI	C.LUI rd,imm	LUI rd,imm
	MoVe	CR	C.MV rd,rs1	ADD rd,rs1,x0
Shifts	Shift Left Imm	CI	C.SLLI rd,imm	SLLI rd,rd,imm
Branches	Branch=0	CB	C.BEQZ rs1',imm	BEQ rs1,x0,imm
	Branch≠0	CB	C.BNEZ rs1',imm	BNE rs1,x0,imm
Jump & Link	J&L	CJ	C.J imm	JAL x0,imm
	Jump & Link Register	CR	C.JALR rd,rs1	JALR rd,rs1,0
System	Sys BREAK	CI	C.SBREAK	SBREAK

32-bit Formats



16-bit Formats

RVM Multiply-Divide Instruction Extension

Category	Name	Format	RV32M (Multiply-Divide)	+RV64	+RV128
Multiply	MULtiply	R	MUL rd,rs1,rs2	MULW rd,rs1,rs2	MULD rd,rs1,rs2
	MULtiply upper Half	R	MULH rd,rs1,rs2		
	MULtiply Half Sign/Uns	R	MULHSU rd,rs1,rs2		
	MULtiply upper Half Uns	R	MULHU rd,rs1,rs2		
Divide	DIVide	R	DIV rd,rs1,rs2	DIVW rd,rs1,rs2	DIVD rd,rs1,rs2
	DIVide Unsigned	R	DIVU rd,rs1,rs2		
Remainder	REMainder	R	REM rd,rs1,rs2	REMW rd,rs1,rs2	REMD rd,rs1,rs2
	REMainder Unsigned	R	REMU rd,rs1,rs2	REMUW rd,rs1,rs2	REMUD rd,rs1,rs2

RVA Atomic Instruction Extension

Category	Name	Format	RV32A (Atomic)	+RV64	+RV128
Load	Load Reserved	R	LR.W rd,rs1	LR.D rd,rs1	LR.Q rd,rs1
Store	Store Conditional	R	SC.W rd,rs1,rs2	SC.D rd,rs1,rs2	SC.Q rd,rs1,rs2
Swap	SWAP	R	AMOSWAP.W rd,rs1,rs2	AMOSWAP.D rd,rs1,rs2	AMOSWAP.Q rd,rs1,rs2
Add	ADD	R	AMOADD.W rd,rs1,rs2	AMOADD.D rd,rs1,rs2	AMOADD.Q rd,rs1,rs2
Logical	XOR	R	AMOXOR.W rd,rs1,rs2	AMOXOR.D rd,rs1,rs2	AMOXOR.Q rd,rs1,rs2
	AND	R	AMOAND.W rd,rs1,rs2	AMOAND.D rd,rs1,rs2	AMOAND.Q rd,rs1,rs2
	OR	R	AMOOR.W rd,rs1,rs2	AMOOR.D rd,rs1,rs2	AMOOR.Q rd,rs1,rs2
Min/Max	MINimum	R	AMOMIN.W rd,rs1,rs2	AMOMIN.D rd,rs1,rs2	AMOMIN.Q rd,rs1,rs2
	MAXimum	R	AMOMAX.W rd,rs1,rs2	AMOMAX.D rd,rs1,rs2	AMOMAX.Q rd,rs1,rs2
	MINimum Unsigned	R	AMOMINU.W rd,rs1,rs2	AMOMINU.D rd,rs1,rs2	AMOMINU.Q rd,rs1,rs2
	MAXimum Unsigned	R	AMOMAXU.W rd,rs1,rs2	AMOMAXU.D rd,rs1,rs2	AMOMAXU.Q rd,rs1,rs2

Three Floating-Point Instruction Extensions: RVF, RVD, & RVQ

Category	Name	Format	RV32{F,D,Q} (SP,DP,QP Fl. Pt.)	+RV64	+RV128
Load	Load	I	FL{W,D,Q} rd,rs1,imm		
Store	Store	S	FS{W,D,Q} rs1,rs2,imm		
Arithmetic	ADD	R	FADD.{S,D,Q} rd,rs1,rs2		
	SUBtract	R	FSUB.{S,D,Q} rd,rs1,rs2		
	MULtiply	R	FMUL.{S,D,Q} rd,rs1,rs2		
	DIVide	R	FDIV.{S,D,Q} rd,rs1,rs2		
	SQuare RooT	R	FSQRT.{S,D,Q} rd,rs1		
Mul-Add	Multiply-ADD	R4	FMADD.{S,D,Q} rd,rs1,rs2,rs3		
	Multiply-SUBtract	R4	FMSUB.{S,D,Q} rd,rs1,rs2,rs3		
	Negative Multiply-SUBtract	R4	FNMSUB.{S,D,Q} rd,rs1,rs2,rs3		
	Negative Multiply-ADD	R4	FNMADD.{S,D,Q} rd,rs1,rs2,rs3		
Move	Move from Integer	R	FMV.S.X rd,rs1	FMV.D.X rd,rs1	FMV.Q.X rd,rs1
	Move to Integer	R	FMV.X.S rd,rs1	FMV.X.D rd,rs1	FMV.X.Q rd,rs1
Sign Inject	SiGN source	R	FSGNJ.{S,D,Q} rd,rs1,rs2		
	Negative SiGN source	R	FSGNJN.{S,D,Q} rd,rs1,rs2		
	Xor SiGN source	R	FSGNJX.{S,D,Q} rd,rs1,rs2		
Min/Max	MINimum	R	FMIN.{S,D,Q} rd,rs1,rs2		
	MAXimum	R	FMAX.{S,D,Q} rd,rs1,rs2		
Compare	Compare Float =	R	FEQ.{S,D,Q} rd,rs1,rs2		
	Compare Float <	R	FLT.{S,D,Q} rd,rs1,rs2		
	Compare Float ≤	R	FLE.{S,D,Q} rd,rs1,rs2		
Convert	Convert from Int	R	FCVT.{S,D,Q}.W rd,rs1	FCVT.{S,D,Q}.L rd,rs1	FCVT.{S,D,Q}.T rd,rs1
	Convert from Int Unsigned	R	FCVT.{S,D,Q}.WU rd,rs1	FCVT.{S,D,Q}.LU rd,rs1	FCVT.{S,D,Q}.TU rd,rs1
	Convert to Int	R	FCVT.W.{S,D,Q} rd,rs1	FCVT.L.{S,D,Q} rd,rs1	FCVT.T.{S,D,Q} rd,rs1
	Convert to Int Unsigned	R	FCVT.WU.{S,D,Q} rd,rs1	FCVT.LU.{S,D,Q} rd,rs1	FCVT.TU.{S,D,Q} rd,rs1
Categorization	Classify Type	R	FCLASS.{S,D,Q} rd,rs1		
Configuration	Read Status	R	FRCSR rd		
	Read Rounding Mode	R	FRRM rd		
	Read Flags	R	FRFLAGS rd		
	Swap Status Reg	R	FSCSR rd,rs1		
	Swap Rounding Mode	R	FSRM rd,rs1		
	Swap Flags	R	FSFLAGS rd,rs1		
	Swap Rounding Mode Imm	I	FSRMI rd,imm		
	Swap Flags Imm	I	FSFLAGSI rd,imm		

Simplicity breeds Contempt

- How can simple ISA compete with industry monsters?
- So far, no evidence more complex ISA justified for general code
  - Cray/RISC were right
- Many advantages to keeping base simple
  - Teaching (what profs do)
  - Learning (what engineers do)
  - Area
  - Energy
  - Quality-of-results versus Design time (HW and SW)
  - Verification
  - Security
  - Extensibility: one base ISA for all customized cores on chip

RISC-V Timeline

- In summer of 2010, UC Berkeley started “3-month project” to develop their own clean-slate ISA
- May 2014, frozen user-level spec (IMAFDQ)
- August 2015, **non-profit RISC-V Foundation** created

Transitioning RISC-V Out of UC Berkeley

- RISC-V Foundation is taking over standards process
  - Incorporated Aug 2015
  - Board of Directors formed Summer 2016
- Tools are starting the upstreaming process
- Students graduating
  - Lead RISC-V devs no longer at UCB
    - new start-up called SiFive
  - But many new students (github.com/ucb-bar)

Foundation Mission Statement

The RISC-V Foundation is a non-profit consortium chartered to standardize, protect, and promote the free and open RISC-V instruction set architecture together with its hardware and software ecosystem for use in all computing devices.

Platinum Founding Members

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bluespec

cortus

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DRAPER

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VectorBlox embedded supercomputing

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Technolution

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  - Professor in the EECS Department at UC Berkeley
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- Frans Sijstermans
  - Vice President Engineering at NVIDIA
- Ted Speers
  - Technical Fellow, Head of Product Architecture for Microsemi's SoC Group

Bi-annual Workshops

- 1st RISC-V workshop Jan 14-15, 2015 in Monterey, CA
  - Sold out: **144** (33 companies & 14 universities)
  - Slides & videos can be found here
- 2nd RISC-V workshop Jun 29-30, 2015 at UC Berkeley
  - Sold out: **120** (30 companies & 20 universities)
  - Slides & videos can be found here
- 3rd RISC-V workshop Jan 5-6, 2016 at Oracle Redwood City, CA
  - Sold out: **157** (42 companies & 26 universities)
  - Slides & videos can be found here
- 4th RISC-V workshop Jul 12-13, at MIT Cambridge, MA
  - Sold out: **252** (63 companies & 42 universities)
  - Slides & videos can be found here

RISC-V Workshop #4 at MIT in Cambridge, MA USA

- 252 attendees from 63 companies and 42 universities

5th RISC-V Workshop – Save the Date

Nov 29th – 30th, 2016

Google Mountain View, CA

Google

Foundation Status

- Articles of Incorporation filed August 2015
  - RISC-V Foundation Corporation is a legal, non-profit operating entity
- Signed on 40+ Founding members
  - shaped the initial by-laws and membership agreements
- Board of Directors formed in Q2 of 2016
  - Ratify Membership Agreement
  - Ratify set of Bylaws
- **This is just the beginning of RISC-V…**

Software Progress

- binutils, gcc
  - ~~"waiting on lawyers"~~, but should be good to go!
- glibc/Linux
  - will upstream after binutils, etc.
- QEMU
  - ucb-bar/riscv-qemu now has user-mode and system-mode
  - currently upstreaming user-mode
- LLVM
  - upstreaming in progress (ask Alex Bradbury)
- Fedora disk images now available
- coreboot
  - "RISC-V is a first class citizen"
- UEFI
- FreeBSD

RISC-V Ecosystem
www.riscv.org

- ***Documentation***
  - User-Level ISA Spec
  - Privileged ISA draft
  - Compressed ISA draft
  - External Debug draft
- ***Software Tools***
  - GCC/glibc/GDB
  - LLVM/Clang
  - Verification Suite
- ***Software***
  - Linux, FreeBSD
  - Yocto
  - Fedora disk images
- ***Software Implementations***
  - QEMU
  - Spike, In-house ISA Sim.
  - ANGEL, JavaScript ISA Sim.
- ***Hardware Implementations***
  - UCB Rocket Chip Generator
    - Rocket in-order core
    - BOOM out-of-order core
  - External implementations
    - PicoRV32
    - Pulp Platform
    - mRISCV
    - and many many more...

RISC-V Summary

- Strong Industry Support
  - 40+ Founding Sponsors
  - Broad commercial and academic interest (252 workshop attendees representing 63 companies & 42 universities)
- Membership & Bylaw documents being ratified
- Board of Directors formed in Q2 2016
- 5th RISC-V Workshop save the date…

Nov 29th – 30th, 2016
Google Mountain View, CA

Isa abierto versus Isa Propietario

- En 2014 los desarrolladores de RISC-V publicaron un articulo en la revista on-line Microprocessor Report donde presentan su propuesta para establecer un estándar abierto de ISA:
  - “The Case for Open Instruction Sets”
  - http://linleygroup.com/mpr/article.php?pub=1&id=11267
- Como contrapartida la misma revista publico un articulo por parte de ingenieros de ARM donde defiende un ISA propietario:
  - “The Case for Licensed Instruction Sets”
  - http://linleygroup.com/mpr/article.php?id=11268