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An ANN-Based High Impedance Fault Detection Scheme: Design and Implementation

Hassan Khorashadi Zadeh*

*University of Birjand, hkhorashadi@yahoo.com

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Abstract

This paper presents a new approach to detection of high impedance faults in distribution systems using artificial neural networks. The proposed neural network, was trained by data from simulation of a distribution system under different faults conditions, and tested by data with different system conditions. The proposed neural network has been implemented on a digital signal processor board and its behavior is investigated on a computer power system model. Details of the design procedure, implementation and the results of performance studies with the proposed relay are given in this paper. Performance studies results show that the proposed algorithm performs very well in detecting a high impedance fault with nonlinear arcing resistance. It is clearly shown that with this integrated approach, the accuracy in fault detection is significantly improved compared to other techniques based on conventional algorithms.

KEYWORDS: High impedance faults, distribution system and artificial neural network

1. INTRODUCTION

Detection and identification of High Impedance Faults (HIF) in electrical distribution networks are a challenge for protection engineers. This is due to the nature of this kind of faults and their variability and relatively low fault current levels with respect to feeder load current. HIF in power networks represent safety hazards, utility liability problems and possible equipment and property damage due to arcing and resistance fires.

Various schemes and algorithms have been proposed by different researchers to cope with the problems associated with HIF. HIFs are extremely difficult to be cleared by conventional over-current protection due to low current involved. Most conventional fault detection techniques for HIF mainly involve processing information based on the feature extraction of post-HIF current and voltage signals [1]. Some of the proposed detection schemes employ various algorithms such as digital signal processing [2], high frequency noise power spectra [3], expert system [4, 5] and wavelet transform [6-8]. These algorithms are proposed as solutions to the misdetection and false detection problems associated with the currently present algorithms. Each of these techniques could improve fault detection, but each has its drawback as well.

HIF relay mal-operation could be caused during some transient events such as feeder energization, load switching and capacitor bank switching. Nonlinear solid-state loads such as computers, uncontrolled and controlled rectifiers, lighting controls and variable speed motor drives could also produce excessive levels of harmonics and ripples in the power spectra in the range of 100–10000 Hz. These harmonics might be classified as a HIF event by the high impedance fault detection algorithm.

Protective relaying is just as much a candidate for the application of pattern recognition techniques. The majority of power system protection techniques are involved in defining the system state through identifying the pattern of the associated voltage and current waveforms measured at the relay location. This means that the development of adaptive protection can be essentially treated as a problem of pattern recognition/classification. Artificial Intelligence (AI) based algorithms including neural networks are powerful in pattern recognition and classification. They possess excellent features such as generalization capability, noise immunity, robustness and fault tolerance. Consequently, the decision made by an AI-based relay would not be seriously affected by variations in system parameters. AI-based techniques have been used in power system protection and encouraging results are obtained [9].

AI based detection and classification schemes offer one of the best alternatives to the HIF problem as they provide well trained noise tolerant detection

algorithms with the potential of training and retraining using actual field HIF fault data. Some of the published articles dealing with the application of ANN in protective relaying are related to the high impedance fault detection [10]–[13]. Some of power system conditions produce transient signals, which may look similar to those of high impedance faults in frequency domain. Most of these approaches have not investigated these transients.

In this application, capabilities of neural networks are used to identify high impedance faults in electrical distribution networks. Design and hardware implementation of a Neural Network (NN) based approach for an accurate HIF detection algorithm is presented in this paper. Application of the proposed algorithm reduces the effect of system variables such as fault resistance and source impedance on the decision made by the HIF relay. It is shown that the proposed relay is able to accurately distinguish between high impedance faults and other cases such as load and/or capacitance switching. The proposed algorithm is tested to evaluate its performance in terms of accuracy and robustness. Some of the test results are included in the paper.

2. FAULT SIMULATION

2.1 Nonlinear Arc Resistance Model

There have been many studies in the field of arcing and ground resistance [14, 15, 16]. Continuous conduction of a fault arc requires a certain amount of voltage gradient to be applied. Research shows that the voltage across the arc has a flattop waveform [16]. The magnitude of the arc voltage may vary depending on arc length but it is independent of current through the arc. For example, in a simple distribution system the current through the arc is determined only by source voltage and fault loop impedance because the arcing resistance R_f is small.

The high impedance faults were simulated using the transformer model reported in [11]. This HIF model, as shown in Fig. 1, consists of a nonlinear resistor, two diodes, and two dc sources that change amplitudes randomly every half cycle. Thus, some dynamics and randomness are represented. Changing the mean and standard deviation of the dc source voltage amplitudes could be used to more closely approximate different ground surfaces such as asphalt, sand, or grass.

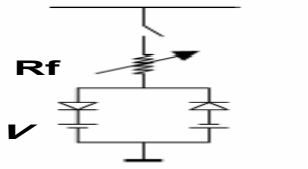

Fig. 1. Nonlinear arcing resistance model

2.2 Power System Model

The training data sets of an ANN were obtained from simulation results based on a typical distribution system as shown in Fig. 2. It depicts the sample study system of two radial distribution feeders with linear and nonlinear loads, voltage correction capacitor banks and equivalent HIF arc model. Since disturbances resulting from HIFs may resemble those from capacitor switching and transformer tap changing, it is therefore necessary to include cases with these contingencies to ensure that the ANNs will not be confounded even under the high level of ambient harmonics so generated.

Digital simulations were performed using an electro-magnetic transient program PSCAD/EMTDC [17] for different types of faults, fault location and other contingencies such as capacitor switching, signal phase load switching, non load transformer switching etc. Combination of different fault conditions considered for training pattern data generation is shown in Table 1.

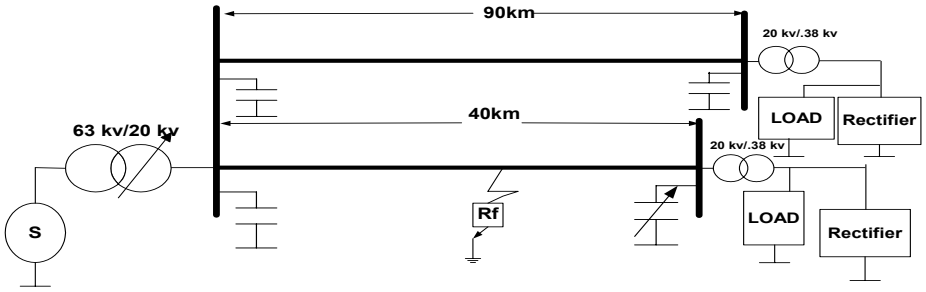

Fig. 2. Simulated system model

Table 1. Training patterns data generation

Fault Location (km)	2,5,7,7.5,9,9.8,10,15,19,21,27,30,33, 35, 37, 40
Arc Voltage (V) (Random)	Different values between (0-5000)
Inception angle (deg)	Different values between (0-360)
C (kVar)	Different values between (0-300)
Tap changer	-4.5, 0, 4.5
Load (MW) (linear-nonlinear)	15,20,30,50

3. DESIGN OF NEURAL NETWORK HIF DETECTOR

In this paper, an ANN-based scheme is proposed as a high impedance fault detection module. The proposed module processes the current and voltage signals

at the relay location at the beginning of the distribution line. Block diagram of the proposed approach is shown in Fig. 3.

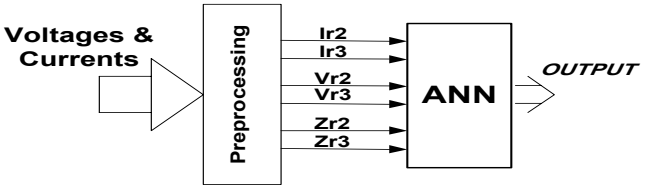

Fig. 3. The proposed algorithm's structure

3.1 Inputs and Outputs

In this study, six input signals are considered at the input layer of the proposed ANN. The neural network processes lower order harmonics of the voltage and current signals. The input signals are prepared at the preprocessing stage.
The six input signals required at the input layer are namely *Ir2, Ir3, Vr2*, *Vr3, Zr2 and Zr3*. *Ir2* and *Ir3* are the second and third harmonics of the residual current. Similarly, *Vr2* and *Vr3* are the second and third harmonics of residual voltage. The residual current and voltage are defined as:

$$\begin{aligned} Ir &= Ia + Ib + Ic \\ Vr &= Va + Vb + Vc \end{aligned} \qquad (1)$$

where V_a , V_b and V_c are the voltages at the relay location and I_a, I_b and I_c are the currents through the relay.

Zr2 and *Zr3* are the second and third harmonics of residual apparent impedance of the faulted distribution line. They are measured at the relay location using (2):

$$\begin{aligned} Zr2 &= \left| \frac{Vr2}{Ir2} \right| \\ Zr3 &= \left| \frac{Vr3}{Ir3} \right| \end{aligned} \qquad (2)$$

The ANN unit processes its six inputs and makes a suitable decision based on the power system state. Its output is activated for a high impedance fault and remains stable for other system states.

3.2 Preprocessing

The process of generating input patterns from the voltages and currents signals is depicted in Fig. 4. Samples of three phase voltages and currents at the relay location obtained from the power system simulated by the EMTDC software. These samples were processed by 2nd order low-pass anti-alising filters and were re-sampled at 1 kHz. The anti-alising filters had a cut-off frequency of 450 Hz.

Samples of the residual current and voltage signals are then obtained using (1). Next the second and third harmonics (of magnitude and angle) of these signals have been obtained using the full cycle Discrete Fourier Transform (DFT) algorithm from voltage and current samples. Finally the second and third harmonics of apparent impedance of the faulted distribution line are calculated using (2).

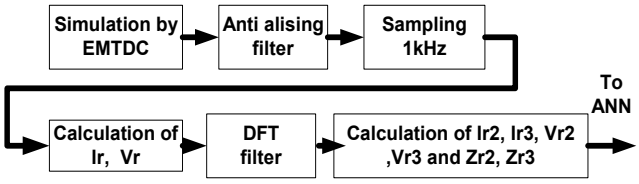

Fig. 4. Pre-processing

3.3 Training

Multilayer feed-forward networks were chosen to process the prepared input data. A few different networks were selected initially. For designing the detector neural network, different networks with 6 inputs and 1 output were considered. This was chosen based on an assumed sampling rate of 20 samples per 50 Hz cycle. The networks' architectures were decided empirically, which involved training and testing different number of networks. The numbers of neurons for the hidden layers are chosen to be 8 and 4 neurons. For all the networks, tan-sigmoid function was used as the activation function of the hidden layer neurons. Saturated linear function was used for the output layer.

Various networks with different number of neurons in their hidden layer were trained with both conventional Back-Propagation (BP) and Marquardt-Levenberg (ML) algorithms [18, 19]. While BP is a steepest descent algorithm, ML algorithm is an approximation to the Newton's method. The ML algorithm is a nonlinear least square algorithm applied to learning of the multilayer perceptrons. It was found that the networks trained with the ML algorithm provide better results compared with the results of the networks trained with the BP algorithm. Therefore, it was decided to use the ML training algorithm for this application.

3.4 Test Results

A validation data set consisting of about 100 different fault types was generated using the distribution system model shown in Fig. 2. The validation set of fault patterns were different than the fault patterns used to train the network. For different faults of the validation set, fault type, fault location, fault inception time, and arc voltage were changed to investigate the effects of these factors on the performance of the proposed algorithm.

The proposed ANN output for two faults with different distribution system conditions is shown in Figs. 5 and 6. For these cases, a fault is applied to the system at 15 ms and the ANN output is shown for the first 25 ms after the fault inception, which is of utmost interest.

The ANN output for a single phase to ground fault CG, is shown in Fig. 5. Fault location was 18km from the relay location, with 2000 V arc voltage. As shown in this figure, the ANN is able to respond to the fault correctly in a timely fashion.

The next example tests the ANN's performance for a fault at another location. Fig. 6 shows the output of the ANN for a fault BG at 7 km from the relay location, with 4000 Varc voltage. The ANN performs correctly and quite fast, as shown in this figure.

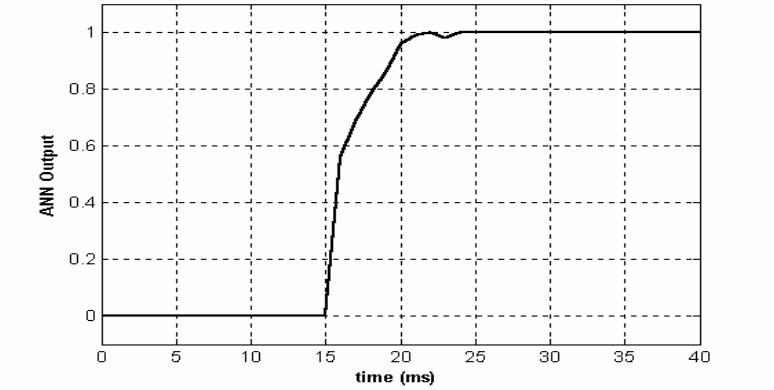

Fig. 5. HIF Detector for CG fault at 18 km and with arc voltage $V_f = 2000$ V

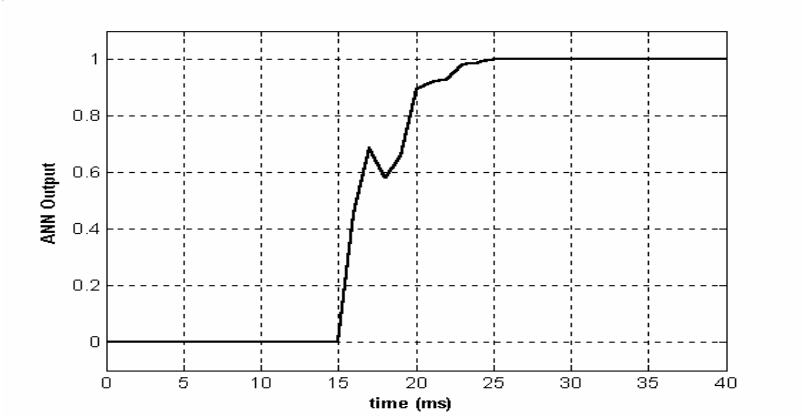

Fig. 6. HIF Detector for BG fault at 7 km and with arc voltage $V_f = 4000$ V

4. IMPLEMENTATION OF THE HIF DETECTOR

The proposed ANN-based HIF detector was implemented on a Digital Signal Processor (DSP) board and its performance was evaluated. In this section, the hardware and software components required for real-time implementation of the proposed HIF detector are described. Details of implementation along with the experimental studies are described as well.

4.1 Hardware System

Appropriate hardware consisting of three cards, namely; minimum system card, Data Acquisition System (DAS) card and Input/Output (I/O) card has been designed to implement the proposed ANN-based algorithm. Hardware configuration of the implemented HIF detector is shown in Fig. 7. Different hardware components are described in the following subsections.

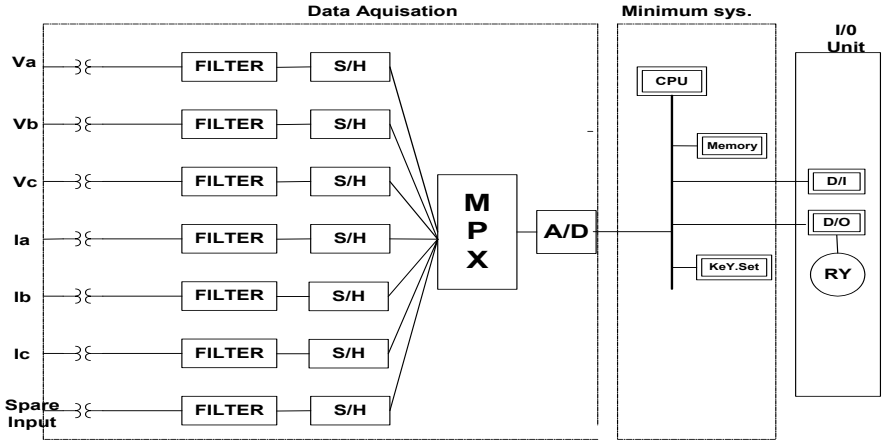

Fig. 7. Hardware configuration of the implemented HIF detector

4.1.1 Minimum System Card

Architecture of the minimum system card is depicted in Fig. 8. This card, based on a 50 MHz TMS320C25 digital signal processor from Texas Instrument [20], is used as a digital signal processor card. This card controls the data-acquisition process. It also processes the acquired signals and implements the proposed technique. As shown in Fig. 8, this card includes 32 Kword EPROM and 8 Kword EEPROM. The designed DSP card includes other features such as Watch-Dog Timer, Keypad and LCD as well.

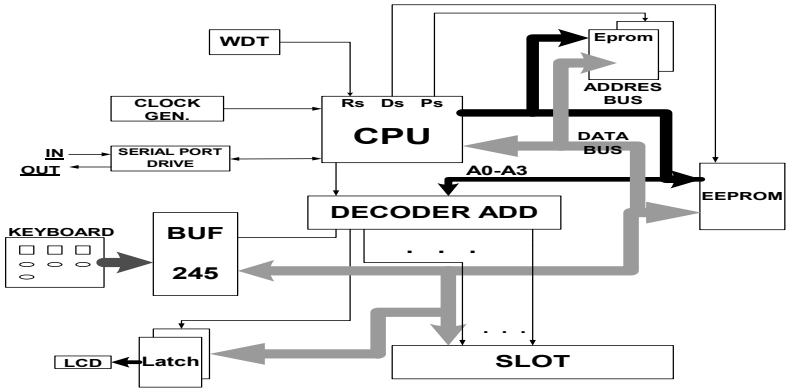

Fig. 8. Configuration of the minimum system card

4.1.2 Data Acquisition Card

Appropriate hardware and software setup for accomplishing data acquisition were designed and fabricated. Active low-pass filters, sample holders, an analog multiplexer and an Analog to Digital (A/D) converter are furnished for sampling and analog-to-digital conversion of the instantaneous voltage and current data. The prepared digital data is then introduced to the minimum system card. Specifications of the components used in data acquisition system are summarized in Table 3.

The sampling frequency f_s used in this work is 1 kHz. To attenuate high frequency components, an array of low-pass filters is used. Designed low-pass filters attenuate 400 Hz component to –20 dB to restrain influence of aliasing and high frequency noise as much as possible. The resolution of the A/D converter is chosen as 12 bits including the sign bit and it has a fast conversion time. Other features of the selected components are provided in Table 2.

Table 2. Specification of the data input system

Circuit	Specification
Active Low-Pass Filter (Anti-Aliasing Filter)	Cut off frequency: 400 Hz Time Delay: 7ms
Sample Holder (S &H)	Acquisition time: 30 Aperture time: 20 ns Hold decay rate: 2 mV/s
Analog Multiplexer (MPX)	Channels numbers: 8 Input ranges: ±10 V
Analog to Digital Converter (A/D)	Resolution: 12 bits (Including sign bit) Conversion time: 20 μs Output code: Two's complement

4.1.3 Input/Output Card

This unit is an interface circuit between digital input/output signals and the relaying logic processor. Nine channels are furnished to be used as inputs and

outputs. Additional I/O boards can also be connected to the I/O channel. Four output relays have been installed on the board. They are used as single phase and three phase trip signals, namely phase A trip, phase B trip, phase C trip and three phase trip. A triac controlled Circuit Breaker (CB) is used for tripping. The breaker has a built-in optical isolation between the power and control circuits providing complete isolation. The breaker operates within one half cycle.

4.2 Software System

Three software packages are required for implementing the prototype relay. These packages include data-acquisition, relaying and user-interface software, all of which have been developed appropriately.

The data-acquisition routine controls a sampling rate timer and acquires samples at successive sampling instances. It consists of two routines: a main routine and an interrupt service routine. The main routine initializes the system cards and sets the timer to achieve a sampling rate of 1000 Hz. Interrupt service routine executes functions related to data-acquisition such as sample and hold, analog to digital conversion and execution of the relaying software.

An executable code of the relaying software has been generated using TMS320 fixed point C compiler and then it is loaded into the DSP memory. Quantized samples obtained from DAS are used by this code to execute the proposed relaying technique. Appropriate programming language has been used to develop the relaying software. Relaying software includes ANN function. The ANN function carries out the computations explained in the previous sections.

A graphical user interface software developed in visual C, uploads the obtained results from the DSP memory. The designed relay settings could also be changed using this interface. The setting program runs in parallel with the main program and changes setting values immediately according to the operator's request.

In addition, the man-machine interface of the designed relay provides the following status information:

1. Key buttons for relaying element selection
2. Four keys for value setting
3. Buttons value displays
4. Setting value displays
5. Relay operation displays
6. Hardware failure alarms

4.3 Experimental Studies

The proposed microprocessor based system employing ANN-based HIF detector algorithm was implemented and tested in the laboratory utilizing the

hardware and software components described in fallowing sections. This section describes the test set-up and some sample test results.

4.3.1 Test Set up and Implementation

Fig. 9 shows an overview of the test set-up. Performance of the proposed ANN-based relay has been verified in real-time using the data obtained through simulating various faults on a meshed 63kV/20kV power system depicted in Fig. 10. The test data is obtained for different power system operation conditions and various types of faults at different locations. Computer simulations are performed using EMTDC software and the obtained data is sent to the designed HIF detector hardware through the computer parallel port and an interface circuit. The prepared data received by the designed hardware is processed and appropriate decision is made based on the designed HIF detector characteristics.

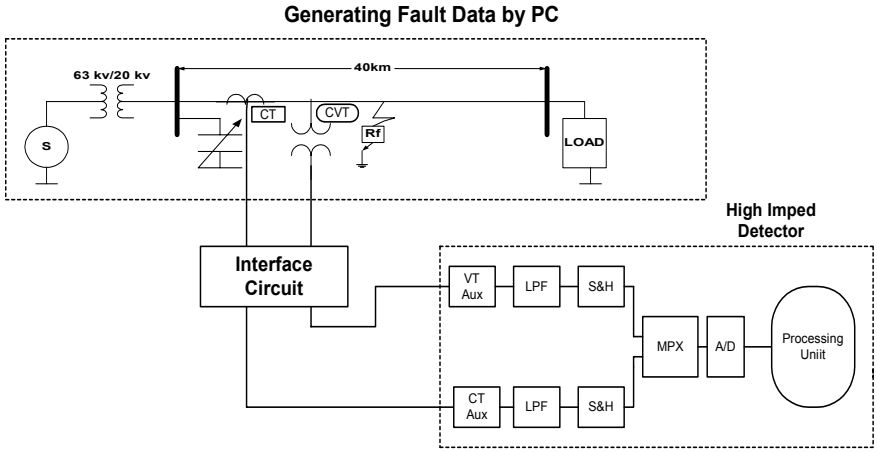

Fig. 9. The block diagram of the test Relay

4.3.2 Real-Time Test Results

The results prove that the purposed detector can easily detect high impedance faults under different conditions and can quickly discriminate HIFs from other transient states as well. Some typical results are demonstrated here.

4.3.2.1 High Impedance Faults

The proposed HIF detector operation for a few faults with different distribution system conditions is presented in Table 4. As an example, test results for a single phase to ground, CG fault at 5 km from the relay location is presented in the first row of the Table 4. The fault inception angle with respect to phase A voltage zero crossing was 60 deg and the bank capacitor was 60 kVar.

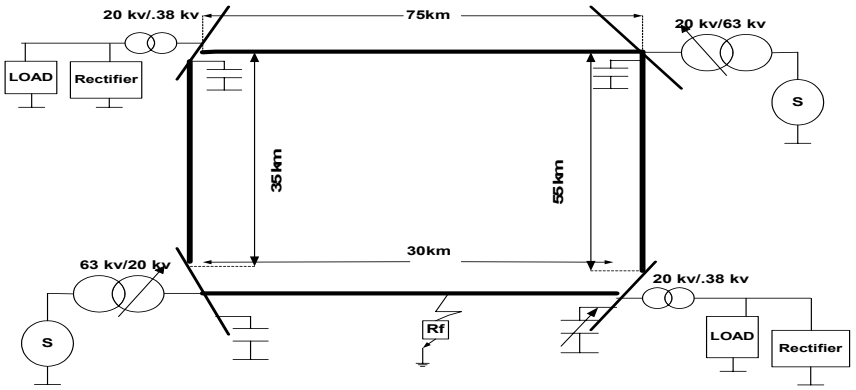

Fig. 10. Simulated meshed power system model

HIF Detector operation for three different amounts of arc voltage is shown in the last three columns of the Table. For the faults, which involve ground, the detector operation for 0V, 2500V and 5000V arc voltage is investigated. As shown in Table 4, the relay performs quite accurately and reliably. The detector output for a few faults with different distribution system conditions is presented in this section. The main emphasis is on checking the network's performance under high impedance fault cases. In general, the ANN performs well and accurate for all fault cases.

Table 4. HIF detector operation test results

Fault Type	Fault Location (km)	θ (°)	C (KVAR)	V_f 0 (V)	V_f 2500 (V)	V_f 5000 (V)
CG	3	30	60	Tr	Tr	Tr
BCG	4.5	50	30	Tr	Tr	Tr
AG	6.8	10	210	Tr	Tr	Tr
BG	7.2	20	40	Tr	Tr	Tr
CG	8.6	50	60	Tr	Tr	Tr
ABG	9.5	40	30	Tr	Tr	Tr
CG	11.5	10	210	Tr	Tr	Tr
BG	14	10	300	Tr	Tr	Tr
ACG	16	100	30	Tr	Tr	Tr
ABG	18	60	200	Tr	Tr	Tr
BCG	20	45	60	Tr	Tr	Tr
ACG	23	-45	100	Tr	Tr	Tr
CG	26	-90	40	Tr	Tr	Tr
BG	28	30	90	Tr	Tr	Tr

(TR): Trip, (-): No Trip, θ : Fault Inception angle, C : Bank Capacitor, V_f: Arc voltage

4.3.2.2 Transient States

Normal capacitor switching operations also produce transient signals, which may look similar to those of high impedance faults in frequency domain, but the results of simulation show that the purposed method is able to discriminate between these transients and high impedance faults. In this study, two kinds of capacitor switching operations are included, one is its energization and another is its de-energization.

Table 5 shows detector operation test results for saturation of capacitor bank de-energization and the capacitor switch on. As shown, the detector has not operated for these states which are similar to high impedance faults.

Table 5. HIF detector operation test results for capacitor switching

Transient state	Changes	HIF Operation
Capacitor Energizing	kVar→ kVar	
	20 → 85	No-Trip
	120 → 240	No-Trip
	240 → 300	No-Trip
	100 → 220	No-Trip
	140 → 200	No-Trip
Capacitor De-energizing	85 → 20	No-Trip
	240 → 120	No-Trip
	300 → 240	No-Trip
	220 → 100	No-Trip
	200 → 140	No-Trip

Results obtained from simulation show that very high frequency contents are usually present during the load switching. Similar to the capacitor switching, distinguishing the HIF from the normal load switching activities is a problem. The purposed HIF detector distinguishes these states from high impedance faults. This matter has been shown in Table 6. In this Table, the output of ANN has been shown for different load switching. As shown, the detector dose not operate for these states.

Table 6. HIF detector operation test results for load switching

	MW→ MW	
Load Switching	23 →25.6	No-Trip
	13.4 → 15	No-Trip
	15 →17	No-Trip
	41 →43.4	No-Trip
	44 →46.7	No-Trip

The operation of power transformers On-Load Tap-Changer (OLTC) produces harmonics and transient signals. The behavior of HIF detector has been surveyed

for operation of OLTC. Table 7 shows the detector operation test results for these transient states. It is shown that detector dose not operate for all these states.

Table 7. HIF detector operation test results for tap changing operation

Transient state	Changes % → %	HIF Operation
Tap Changing	-4.5 → 0	No-Trip
	0 → 4.5	No-Trip
	4.5 → 0	No-Trip
	0 → -4.5	No-Trip

5. CONCLUSIONS

Neural networks, capabilities in pattern recognition and classification are used and a neural network-based HIF detector is designed. The proposed neural network has been implemented on a digital signal processor board. Simulation studies are performed and the relay's performance with different system parameters and conditions is investigated. It results in a more reliable scheme for detection high impedance scheme for distribution lines. It is concluded that neural networks can be used as a part of a new generation of high speed advanced protection relays.

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